



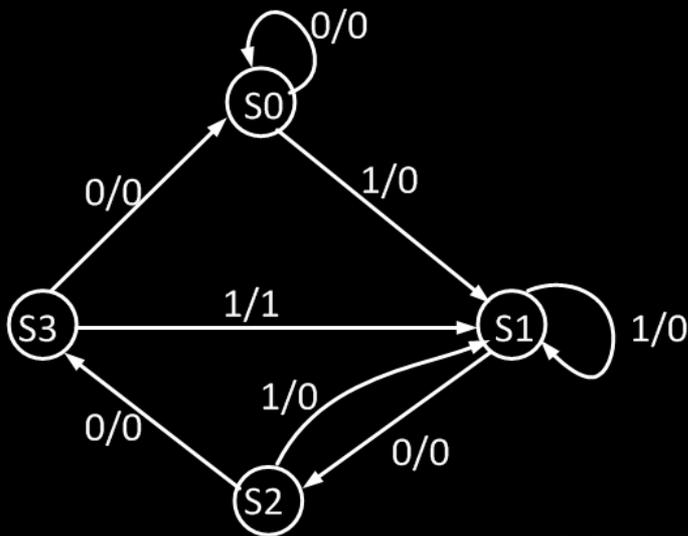
Digital Design

Lecture 20: State Table Reduction

sanjayvidhyadharan.in

Design of Clocked sequential Circuits

Design of sequence detector overlapping (1001)



S0 – 00
 S1 – 01
 S2 – 10
 S3 – 11

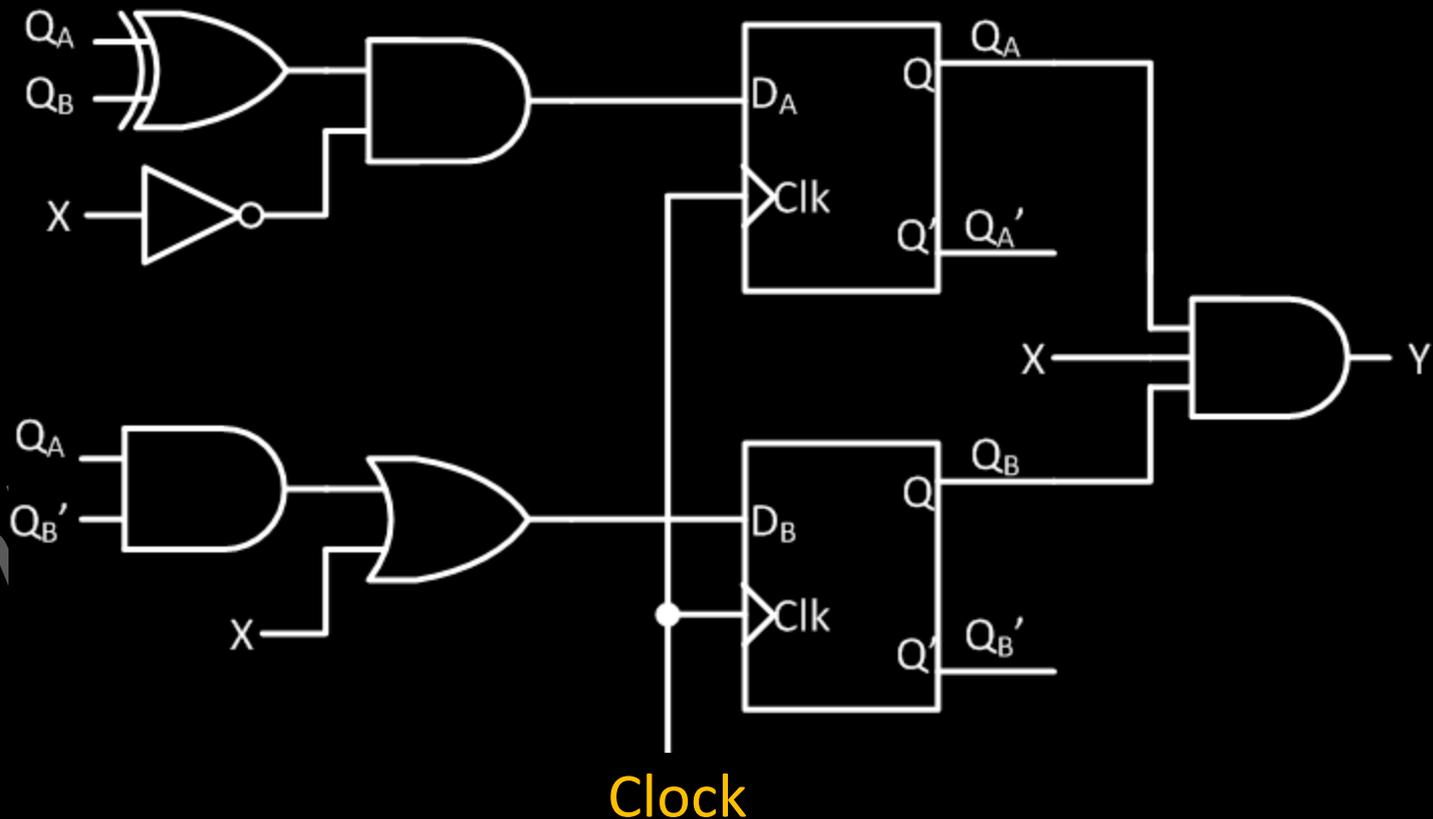
Present State		in		Next State			Out
	Q_A	Q_B	X		$Q_{A(t+1)}$	$Q_{B(t+1)}$	Y
S0	0	0	0	S0	0	0	0
S0	0	0	1	S1	0	1	0
S1	0	1	0	S2	1	0	0
S1	0	1	1	S1	0	1	0
S2	1	0	0	S3	1	1	0
S2	1	0	1	S1	0	1	0
S3	1	1	0	S0	0	0	0
S3	1	1	1	S1	0	1	1

Design of Clocked sequential Circuits

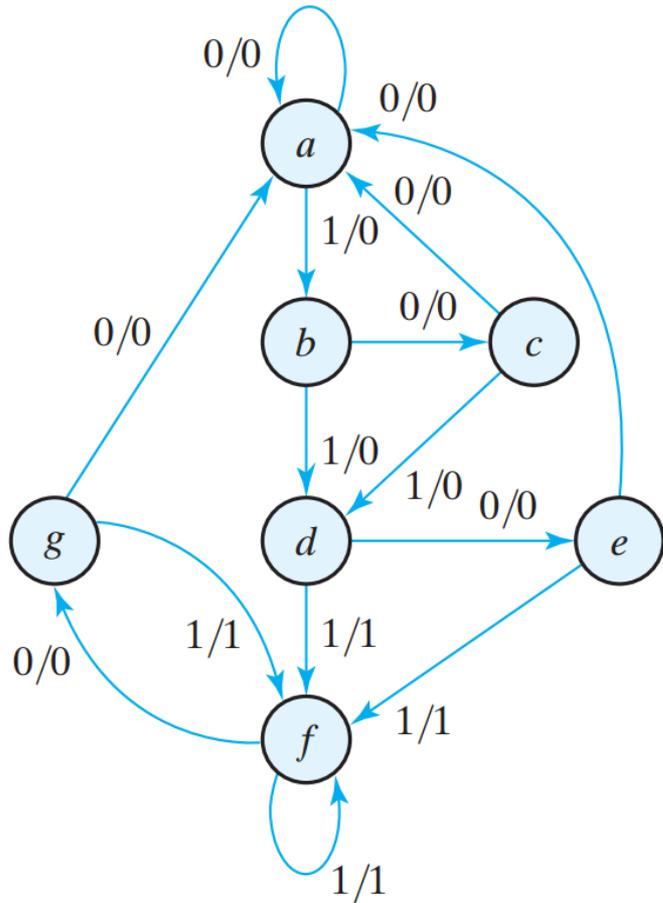
$$D_A = Q_A'Q_BX' + Q_AQ_B'X' = (Q_A \oplus Q_B) X'$$

$$Y = Q_AQ_BX$$

$$D_B = X + Q_AQ_B'$$



State Table Reduction



State Table

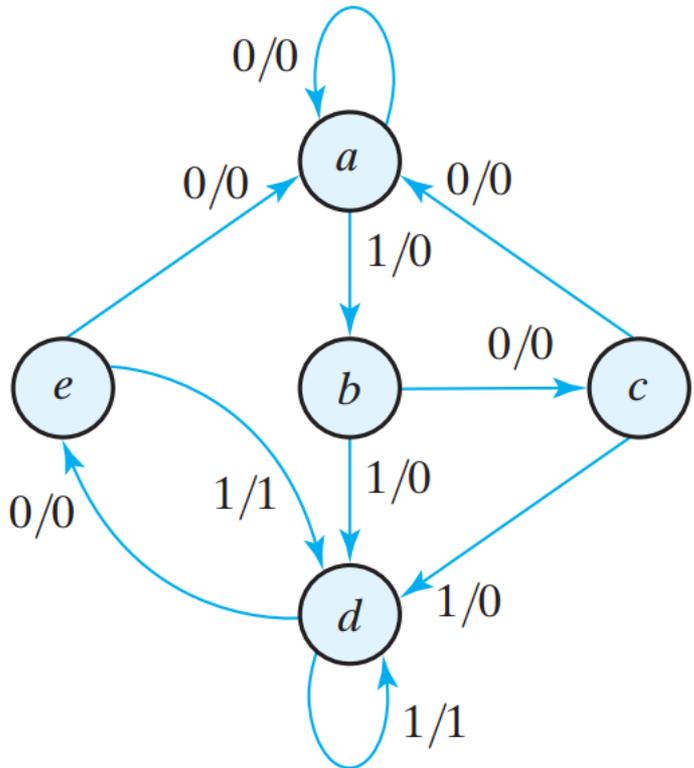
Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
<i>a</i>	<i>a</i>	<i>b</i>	0	0
<i>b</i>	<i>c</i>	<i>d</i>	0	0
<i>c</i>	<i>a</i>	<i>d</i>	0	0
<i>d</i>	<i>e</i>	<i>f</i>	0	1
<i>e</i>	<i>a</i>	<i>f</i>	0	1
<i>f</i>	<i>e</i> ← <i>g</i>	<i>f</i>	0	1
<i>g</i>	<i>a</i>	<i>f</i>	0	1

State Table Reduction

Reducing the State Table

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
<i>a</i>	<i>a</i>	<i>b</i>	0	0
<i>b</i>	<i>c</i>	<i>d</i>	0	0
<i>c</i>	<i>a</i>	<i>d</i>	0	0
<i>d</i>	<i>e</i>	d ← <i>f</i>	0	1
<i>e</i>	<i>a</i>	d ← <i>f</i>	0	1
<i>f</i>	<i>e</i>	<i>f</i>	0	1

State Table Reduction



Reduced State Table

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
<i>a</i>	<i>a</i>	<i>b</i>	0	0
<i>b</i>	<i>c</i>	<i>d</i>	0	0
<i>c</i>	<i>a</i>	<i>d</i>	0	0
<i>d</i>	<i>e</i>	<i>d</i>	0	1
<i>e</i>	<i>a</i>	<i>d</i>	0	1

State Table Reduction

Reduced State Table

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
<i>a</i>	<i>a</i>	<i>b</i>	0	0
<i>b</i>	<i>c</i>	<i>d</i>	0	0
<i>c</i>	<i>a</i>	<i>d</i>	0	0
<i>d</i>	<i>e</i>	<i>d</i>	0	1
<i>e</i>	<i>a</i>	<i>d</i>	0	1

Three Possible Binary State Assignments

State	Assignment 1, Binary	Assignment 2, Gray Code	Assignment 3, One-Hot
<i>a</i>	000	000	00001
<i>b</i>	001	001	00010
<i>c</i>	010	011	00100
<i>d</i>	011	010	01000
<i>e</i>	100	110	10000

Implication Chart

Current State	Next State		Output (Z)	
	$A = 0$	$A = 1$	$A = 0$	$A = 1$
S0	S3	S2	1	1
S1	S0	S4	0	0
S2	S3	S0	1	1
S3	S1	S3	0	0
S4	S2	S1	0	0

State table

Implication Chart

Current State	Next State		Output (Z)	
	$A = 0$	$A = 1$	$A = 0$	$A = 1$
S0	S3	S2	1	1
S1	S0	S4	0	0
S2	S3	S0	1	1
S3	S1	S3	0	0
S4	S2	S1	0	0

State table

S1				
S2				
S3				
S4				
	S0	S1	S2	S3

Implication chart

Implication chart

Implication Chart

S1		x		
S2		✓	x	
S3		x		x
S4		x		x
	S0	S1	S2	S3

(S0,S1)
 (S2,S4)
 (S0,S2)
 (S1,S2)
 (S1,S3)

Implication chart

Current State	Next State		Output (Z)	
	A = 0	A = 1	A = 0	A = 1
S0	S3	S2	1	1
S1	S0	S4	0	0
S2	S3	S0	1	1
S3	S1	S3	0	0
S4	S2	S1	0	0

Current State	Next State		Output (Z)	
	A = 0	A = 1	A = 0	A = 1
S0	S3	S0	1	1
S1	S0	S1	0	0
S3	S1	S3	0	0