



Digital Design

Lecture 18: Sequential Circuit Design

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Sequential Circuits

Design Steps

1. Derive State diagram →
2. State table →
3. State Equations →
4. Circuit

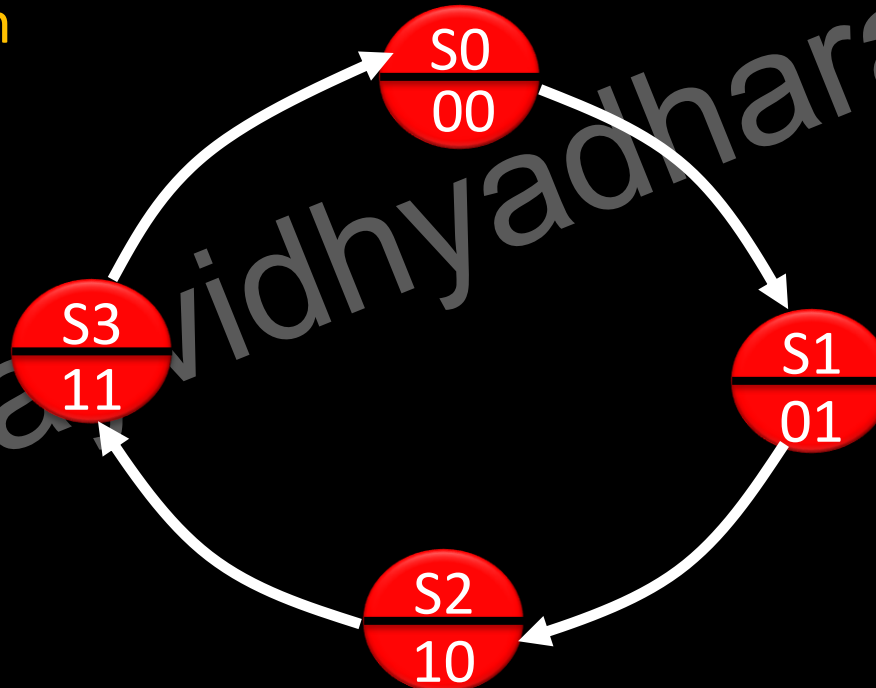
Design of Sequential Circuits

Design

2-bit synchronous counter

Common clock for all the Flip-flops

State Diagram



Sequential Circuits

State Table

Present State			Next State		
	Q_B	Q_A		$Q_B(t+1)$	$Q_A(t+1)$
S0	0	0	S1	0	1
S1	0	1	S2	1	0
S2	1	0	S3	1	1
S3	1	1	S0	0	0



Excitation Tables

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

Characteristic Table

Q(t)	Q(t+1)	J	K	
0	0	0	X	(0 0) (0 1)
0	1	1	X	(1 0) (1 1)
1	0	X	1	(1 1) (0 1)
1	1	X	0	(1 0) (0 0)

Excitation Table

Sequential Circuits

State Table

JK Flip-flop implementation

Present State			Next State			Flip-flop Inputs		Flip-flop Inputs	
	Q_B	Q_A		$Q_B(t+1)$	$Q_A(t+1)$	J_B	K_B	J_A	K_A
S0	0	0	S1	0	1	0	X	1	X
S1	0	1	S2	1	0	1	X	X	1
S2	1	0	S3	1	1	X	0	1	X
S3	1	1	S0	0	0	X	1	X	1

State Equations

$$J_B = Q_A$$

$$K_B = Q_A$$

$$J_A = 1$$

$$K_A = 1$$

Sequential Circuits

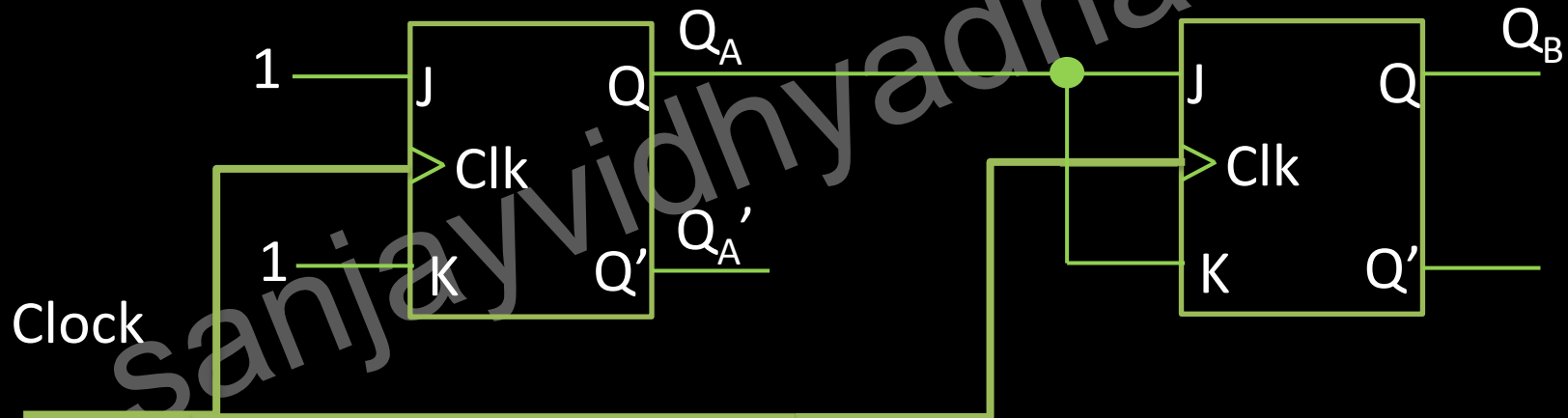
State Equations

$$J_B = Q_A$$

$$K_B = Q_A$$

$$J_A = 1$$

$$K_A = 1$$



Design of Clocked sequential Circuits

D	$Q(t+1)$
0	0
1	1

Characteristic Table

T	$Q(t+1)$
0	$Q(t)$
1	$Q'(t)$

Characteristic Table

$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

Excitation Table

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Table

Sequential Circuits

State Table

D Flip-flop implementation

Present State			Next State			Flip-flop Inputs	
	Q_B	Q_A		$Q_B(t+1)$	$Q_A(t+1)$	D_B	D_A
S0	0	0	S1	0	1	0	1
S1	0	1	S2	1	0	1	0
S2	1	0	S3	1	1	1	1
S3	1	1	S0	0	0	0	0

State Equations

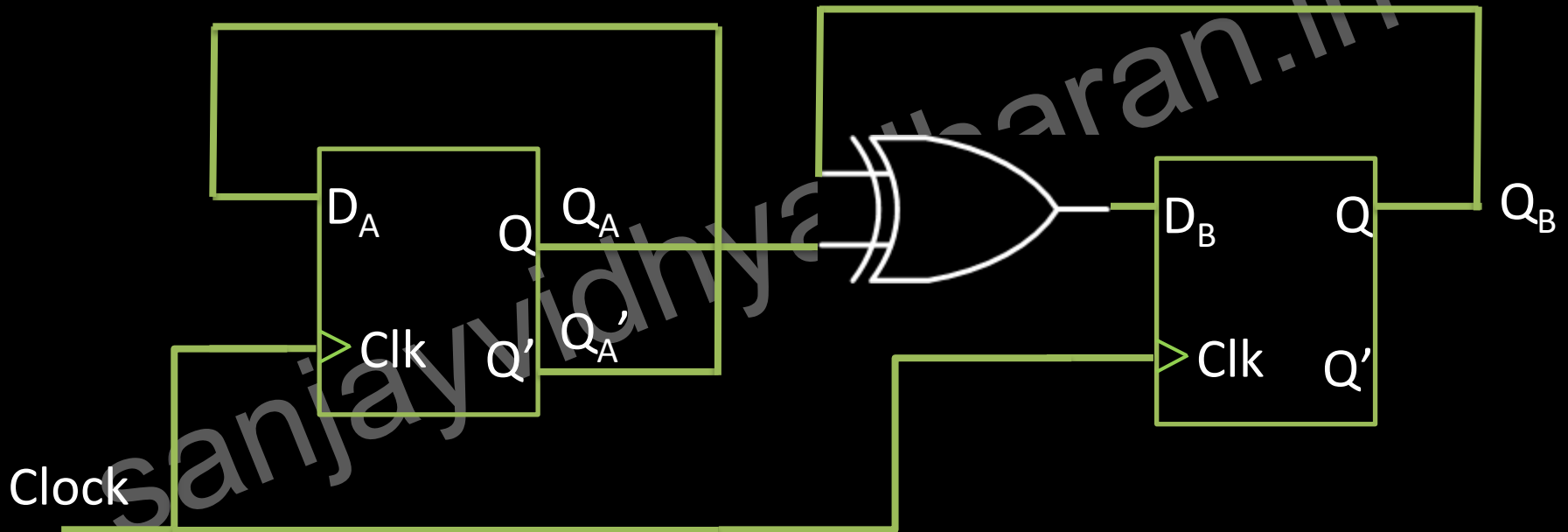
$$Q_B(t+1) = D_B = Q_A \oplus Q_B$$

$$Q_A(t+1) = D_A = Q_A'$$

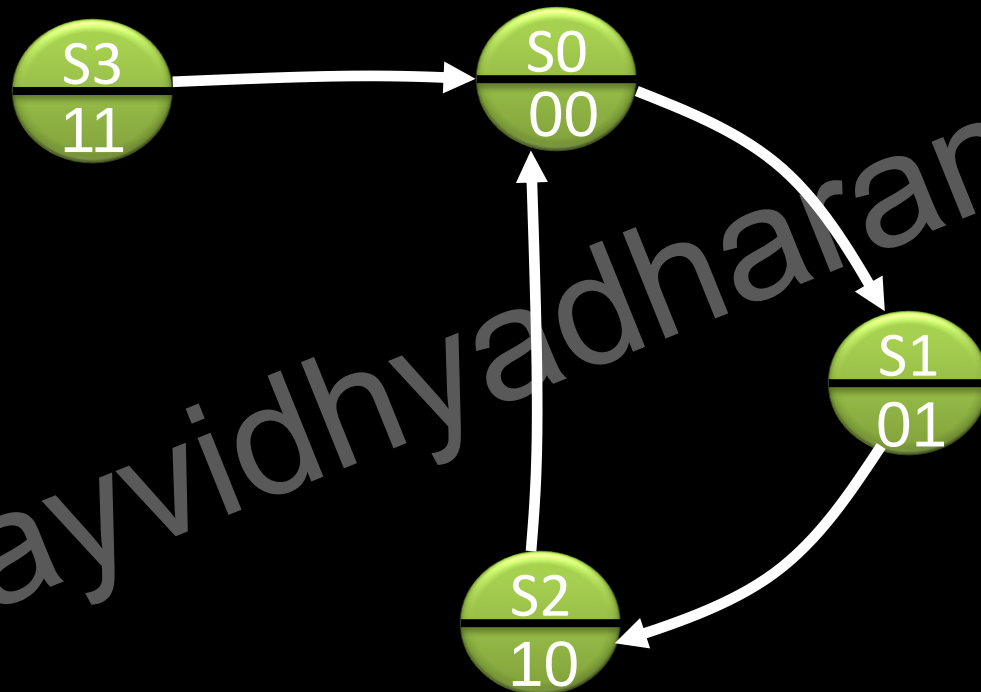
Sequential Circuits

State Equations $Q_B(t+1) = D_B = Q_A \oplus Q_B$

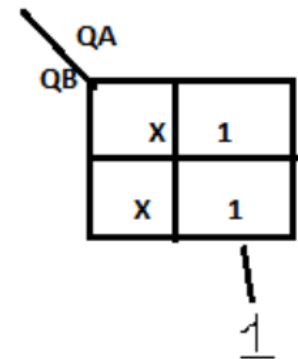
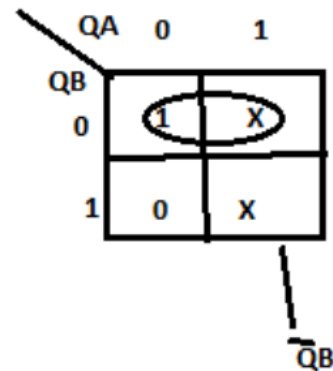
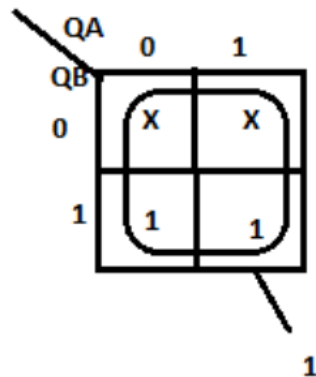
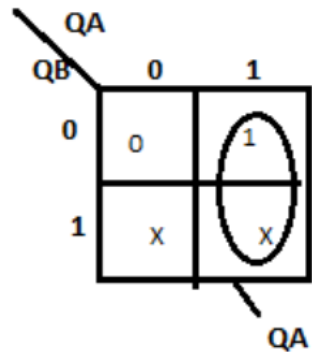
$$Q_A(t+1) = D_A = Q_A'$$



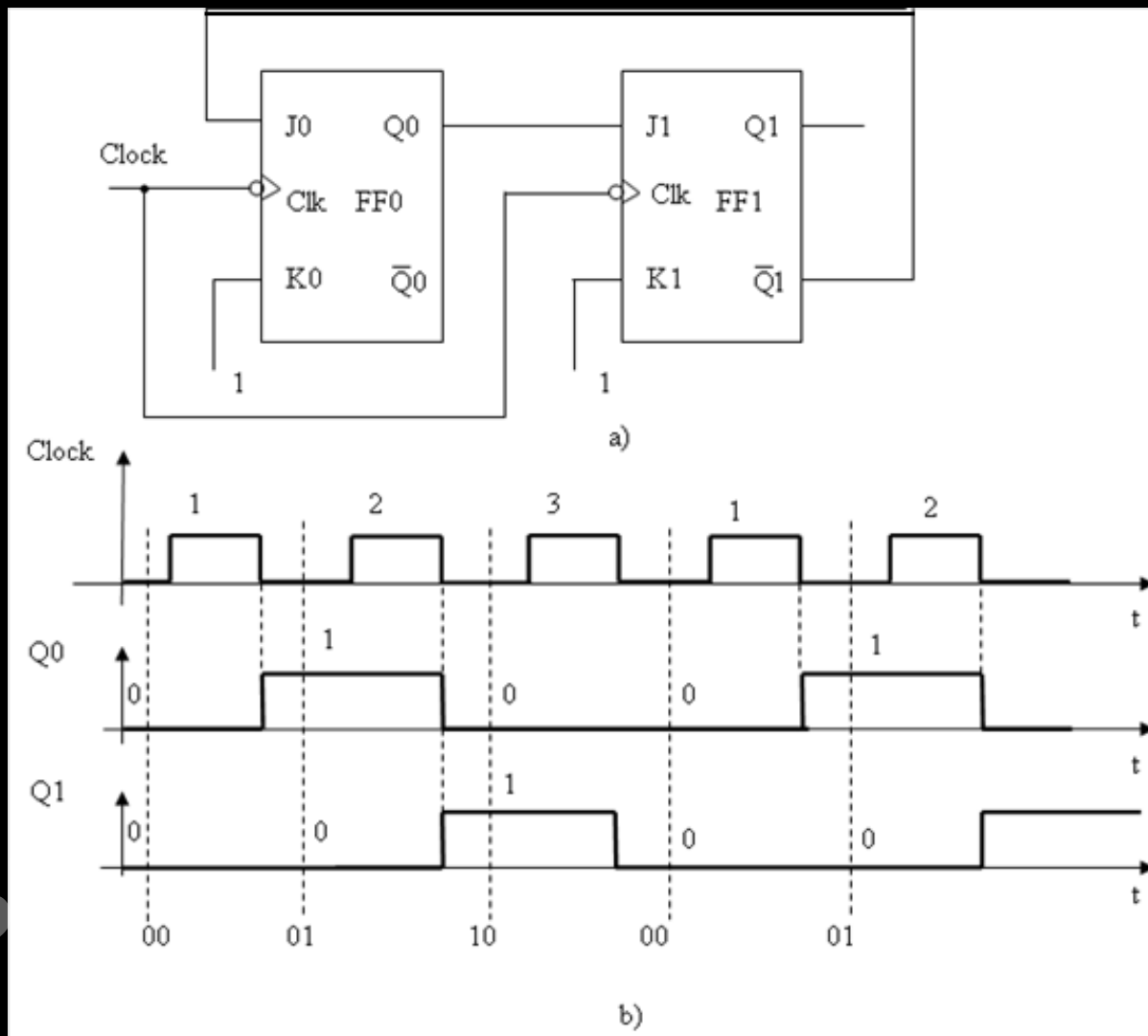
Design Mod 3 synchronous counter



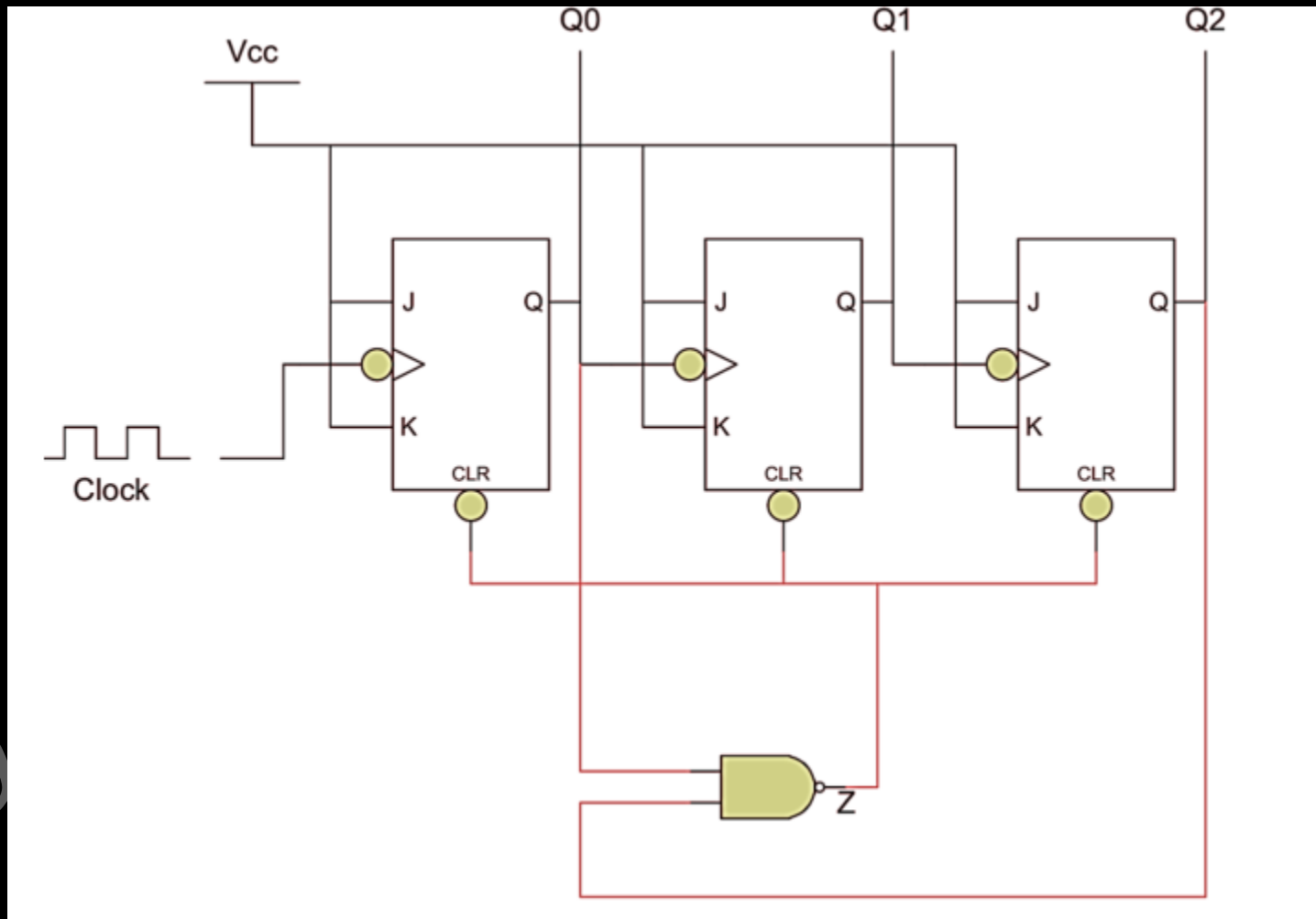
Present states		Next states		Flip-flop Inputs			
Q_B	Q_A	Q_{B+1}	Q_{A+1}	J_B	K_B	J_A	K_A
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	0	0	X	1	0	X
1	1	0	0	X	1	X	1



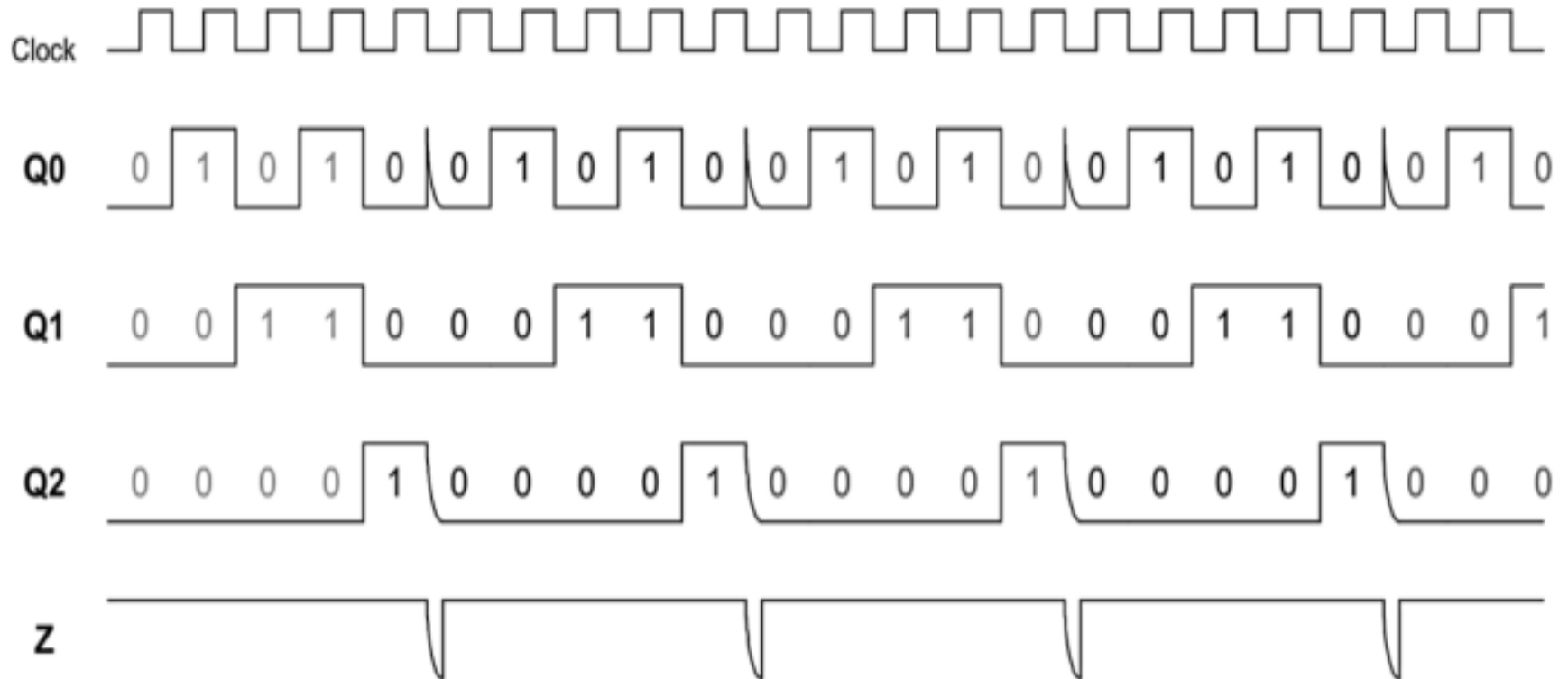
Design Mod 3 synchronous counter



Design Mod 5 Asynchronous counter



Design Mod 5 Asynchronous counter



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Thank You