



Digital Design

Lecture 17: T & JK Flip-Flops

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Digital Electronics and Computer Organization

Digital Design

Lecture 17: T & JK Flip-Flops

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Birla Institute of Technology & Science, Pilani
Hyderabad Campus

2021

Innovate

achieve

2

lead

Flip-Flops interconnection of gates

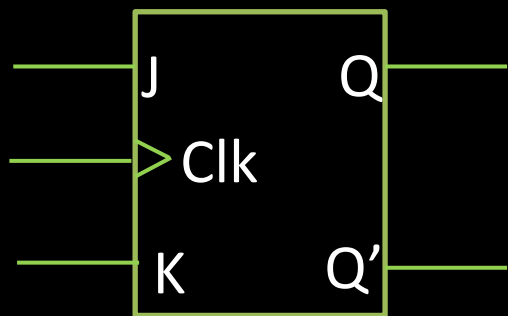
Edge Triggered D Flip-flop – **Most efficient and economical** (less number of gates)

Other Flip-flops

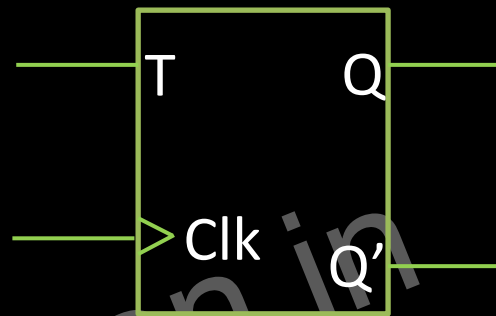
JK Flip-flop

T Flip-flop

Other Flip-Flops



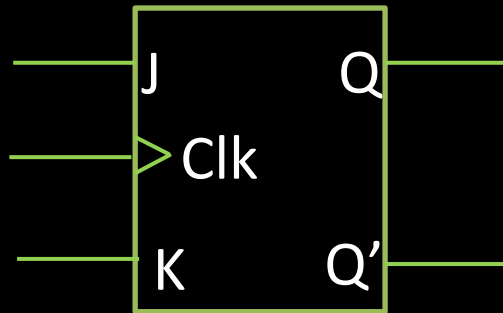
JK Flip-flop



T Flip-flop

Other Flip-Flops

JK Flip-flop



Characteristic Table

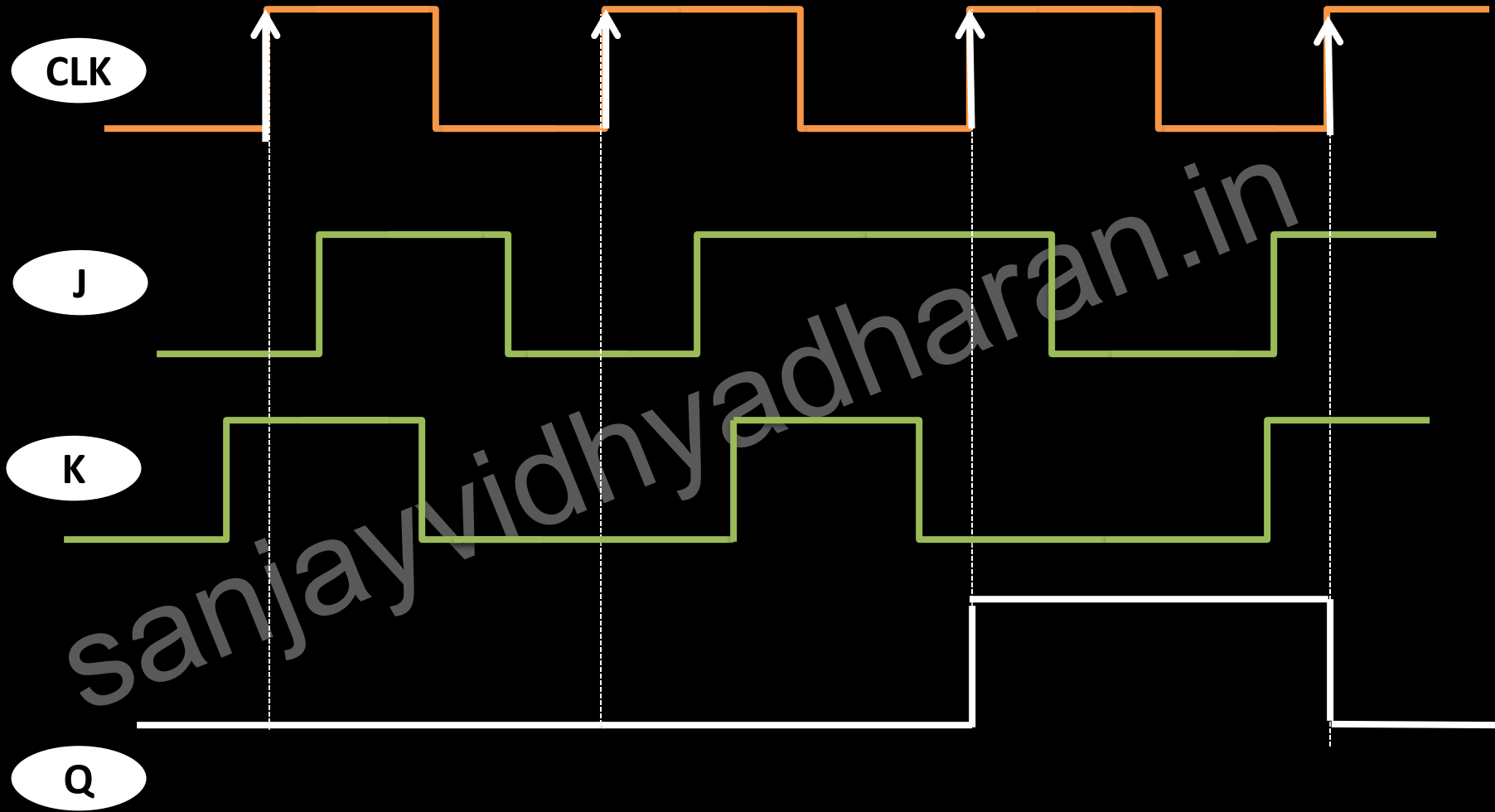
J	K	Q(t+1)	
0	0	Q(t)	No Change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Toggle/ Complement

Characteristic Equation??

$$Q(t+1) = JQ' + K'Q$$

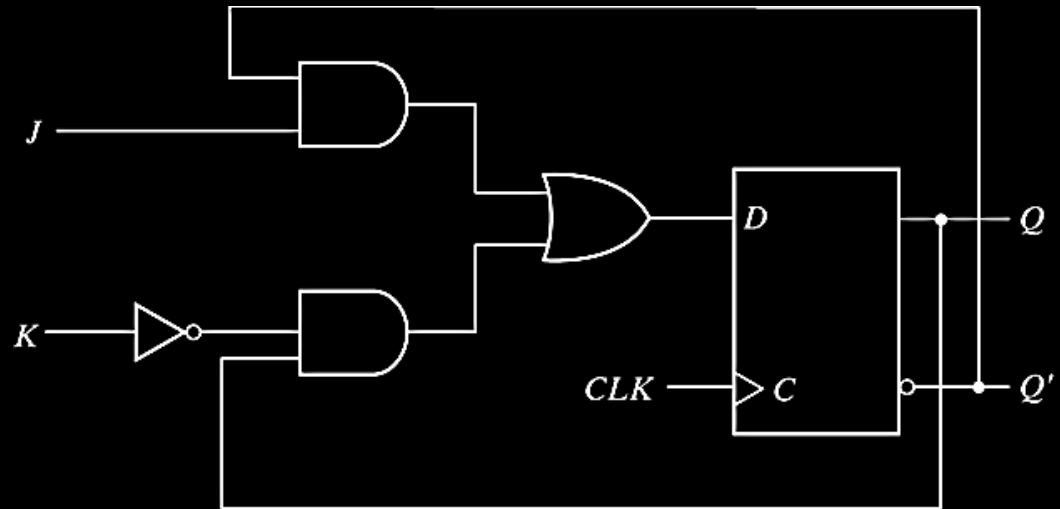
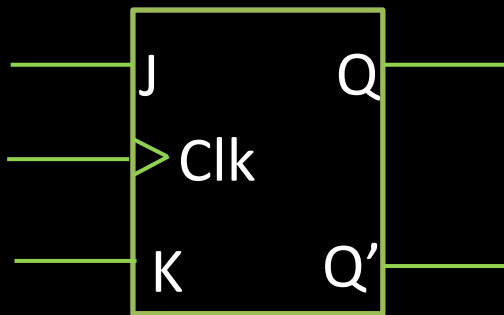
Edge Triggered JK Flip-Flops

Positive Edge triggered



Other Flip-Flops

JK Flip-flop



Design J-K Flip-flop using D flip-flop

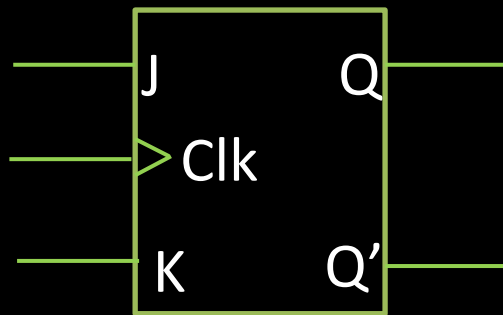
$$Q(t+1) = D$$

$$Q(t+1) = JQ' + K'Q$$

Analyze

Other Flip-Flops

JK Flip-flop



Characteristic Table

J	K	Q(t+1)	
0	0	Q(t)	No Change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Toggle

Characteristic Equation??

$$Q(t+1) = JQ' + K'Q$$

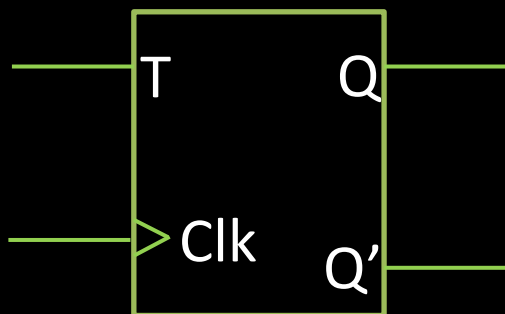
$$Q(t+1) = J'K'.Q + J'K.0 + JK'.1 + JKQ'$$

$$Q(t+1) = J'K'.Q + JK'Q + JK'Q' + JKQ'$$

$$Q(t+1) = K'Q(J' + J) + JQ'(K + K')$$

Other Flip-Flops

T Flip-flop



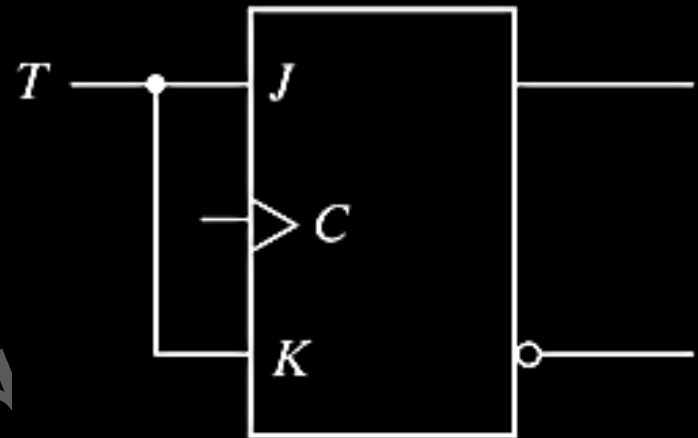
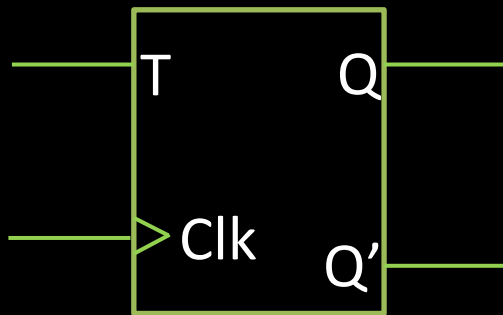
T	Q(t+1)
0	Q(t) No Change
1	Q'(t) Toggle

Characteristic Equation??

$$Q(t+1) = T \oplus Q$$

Other Flip-Flops

T Flip-flop



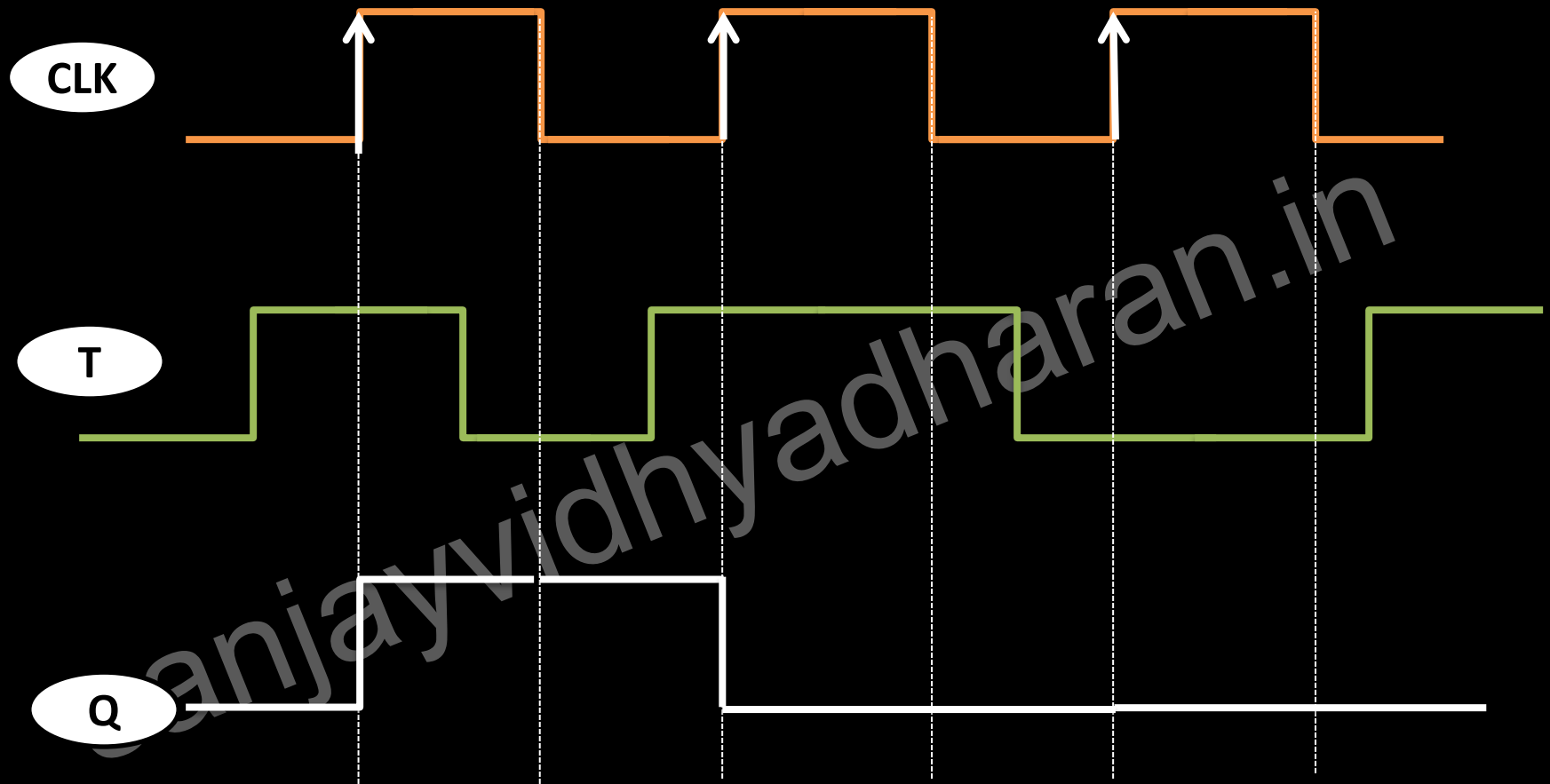
Design T Flip-flop using JK flip-flop

$$Q(t+1) = JQ' + K'Q$$

$$Q(t+1) = T \oplus Q = TQ' + T'Q$$

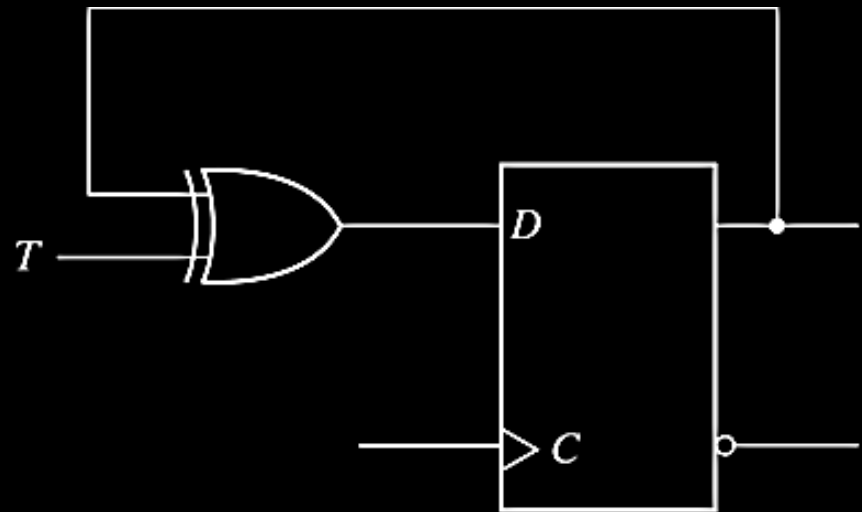
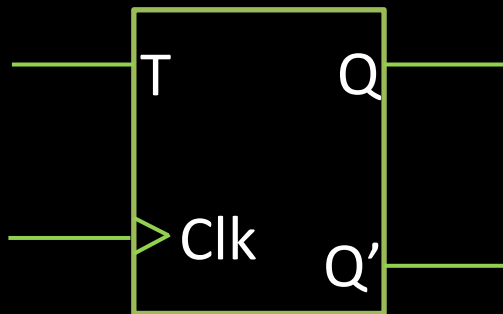
Edge Triggered T Flip-Flops

Positive Edge triggered



Other Flip-Flops

T Flip-flop



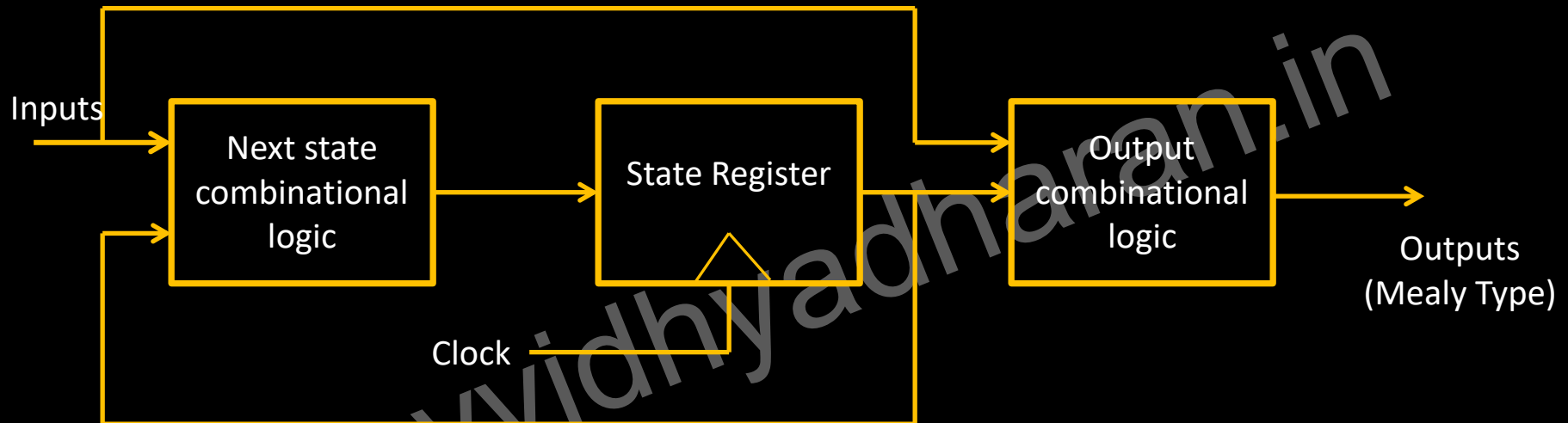
Design T Flip-flop using D flip-flop

$$Q(t+1) = D$$

$$Q(t+1) = T \oplus Q$$

Models of sequential circuits

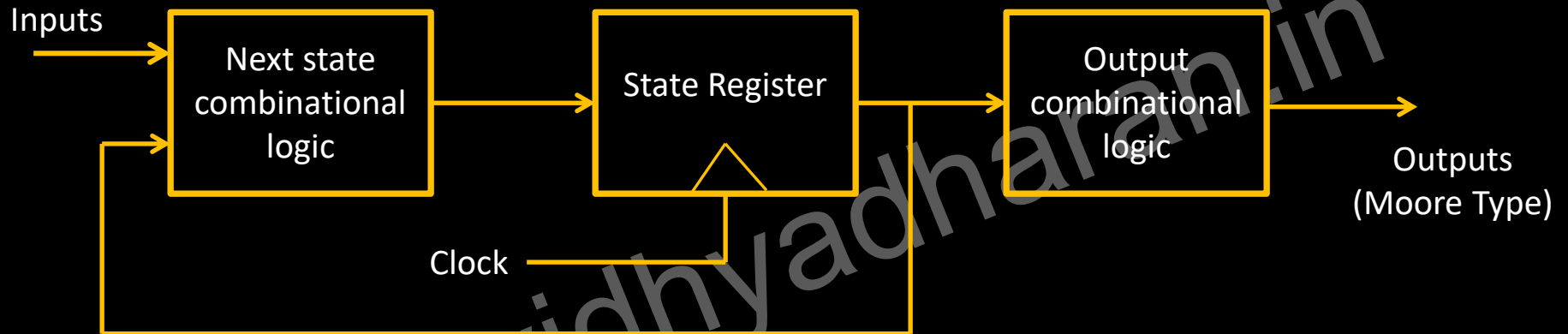
Mealy Model – output depends on present state and input



Outputs change if the inputs change during the clock cycle

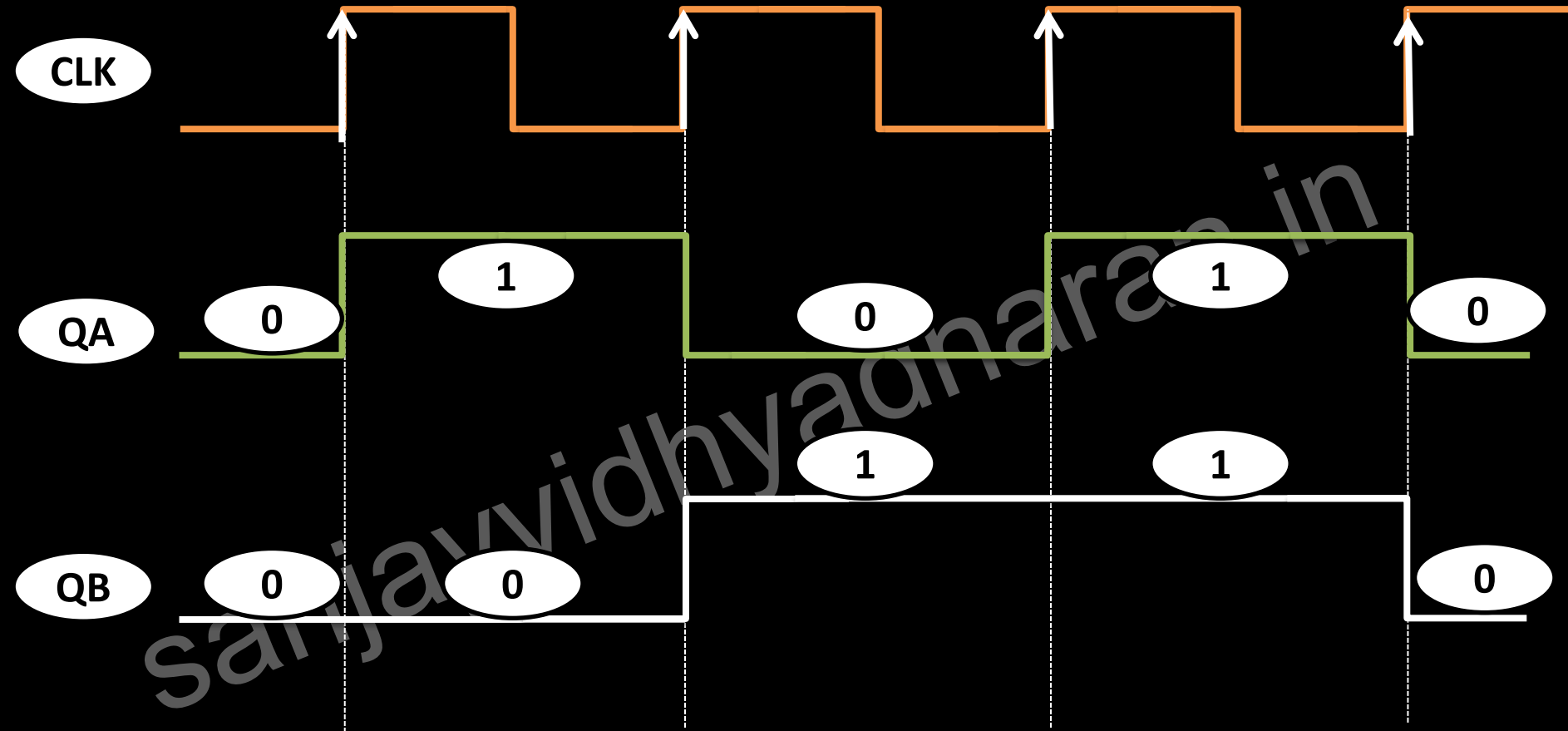
Models of sequential circuits

Moore Model – output depends only on present state only

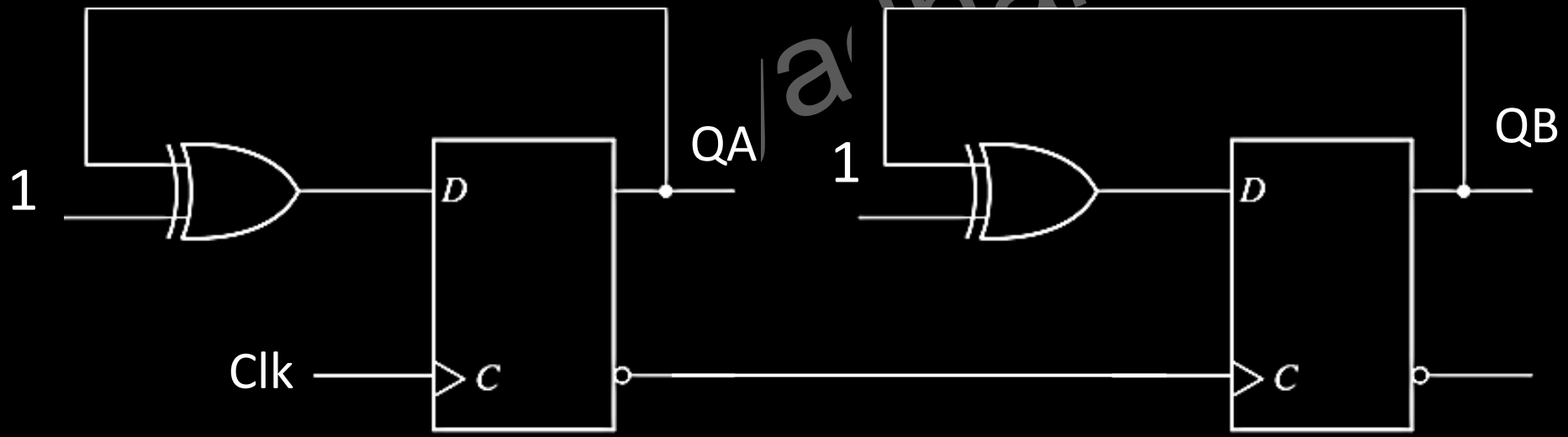
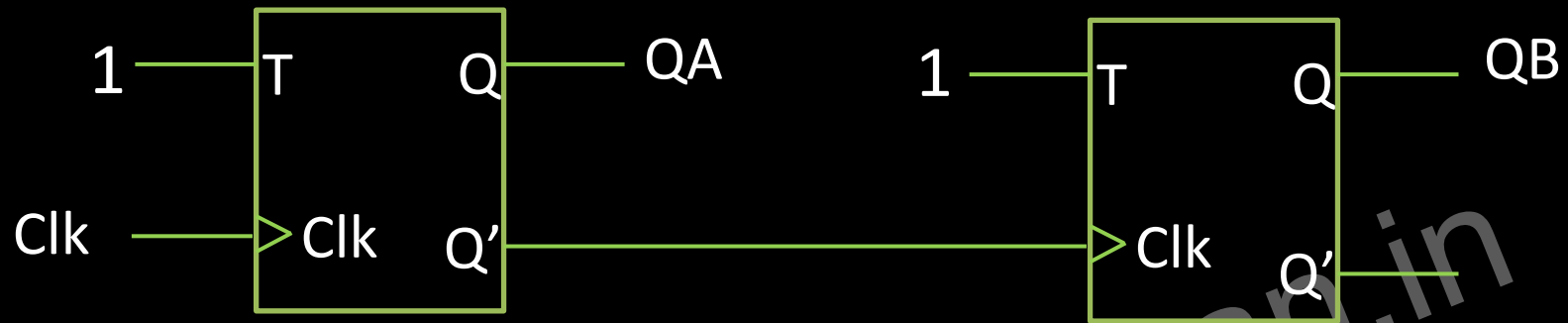


Outputs synchronized with clock

Counter



Asynchronous Counter



Thank You

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