



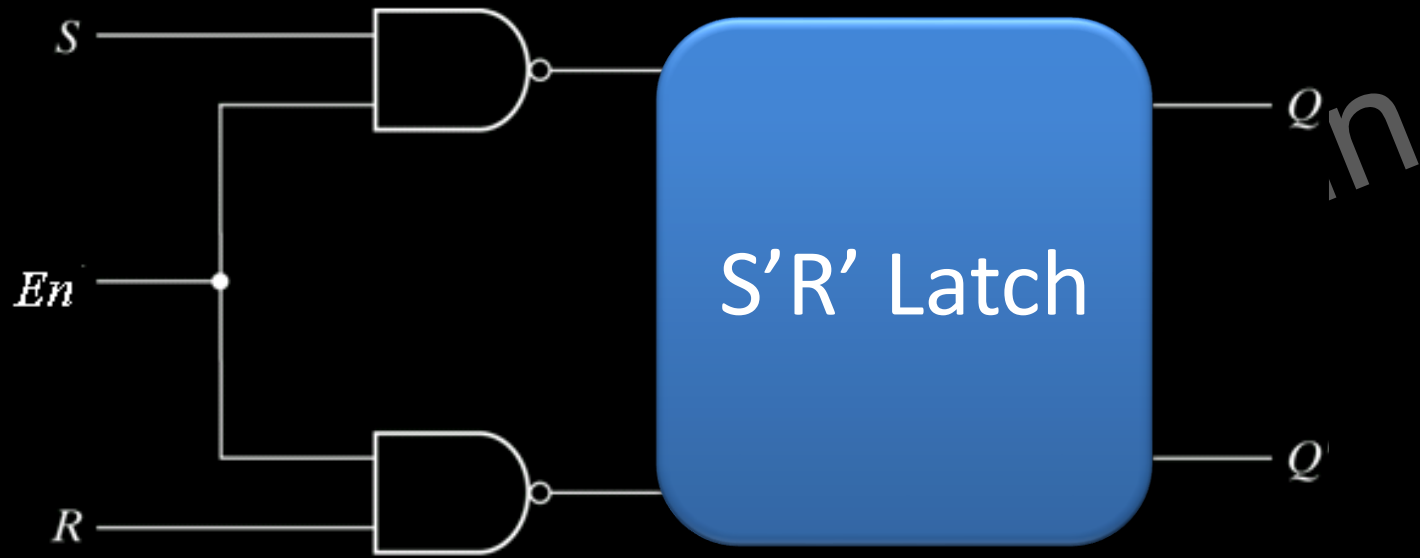
Digital Design

Lecture 16: D-Latches and D-Flipflops

sarijayvidhyadharan.in

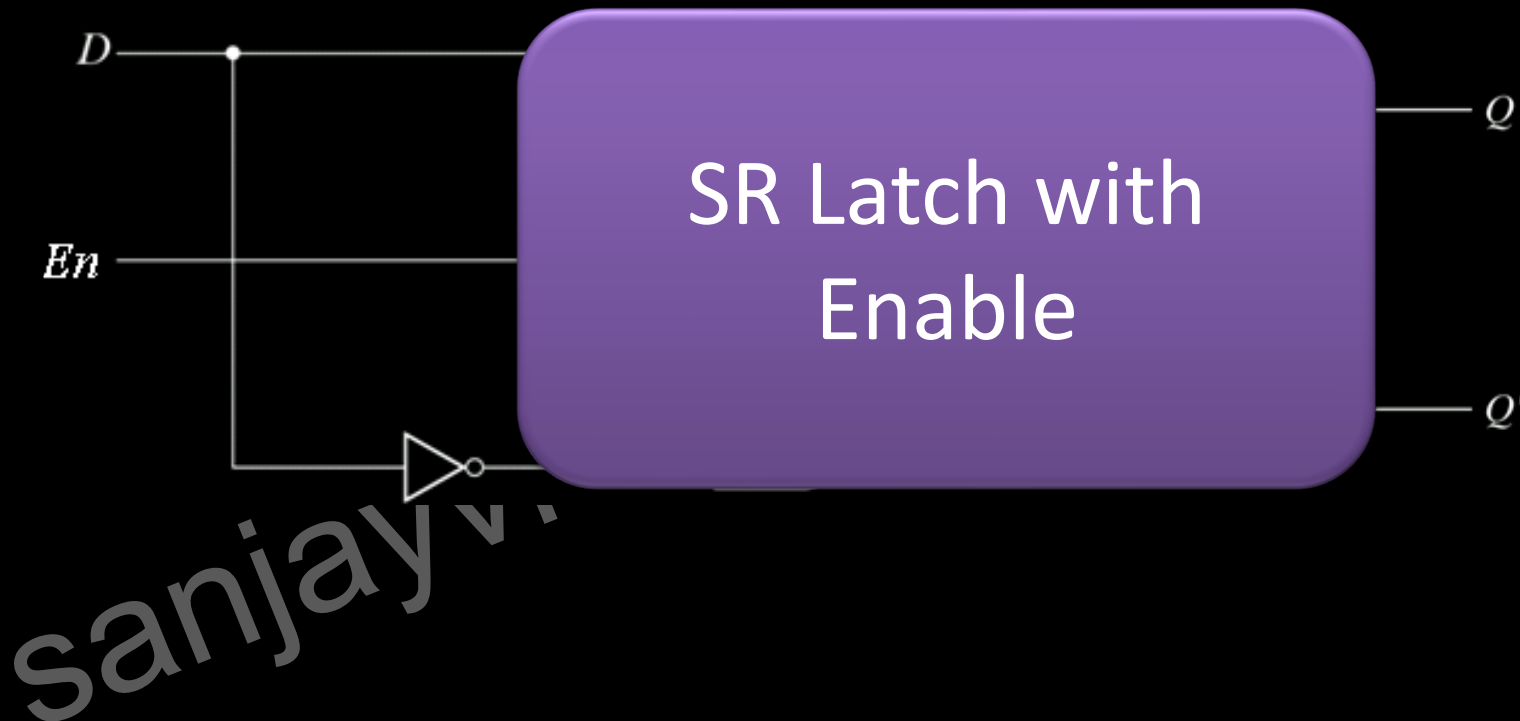
Latches

SR Latch with Enable



Latches

D Flip-flop circuit



Latches

D Latch with Enable

En	D	Q	Q'
0	X	Q	Q'
1	0	0	1
1	1	1	0

No change

Reset

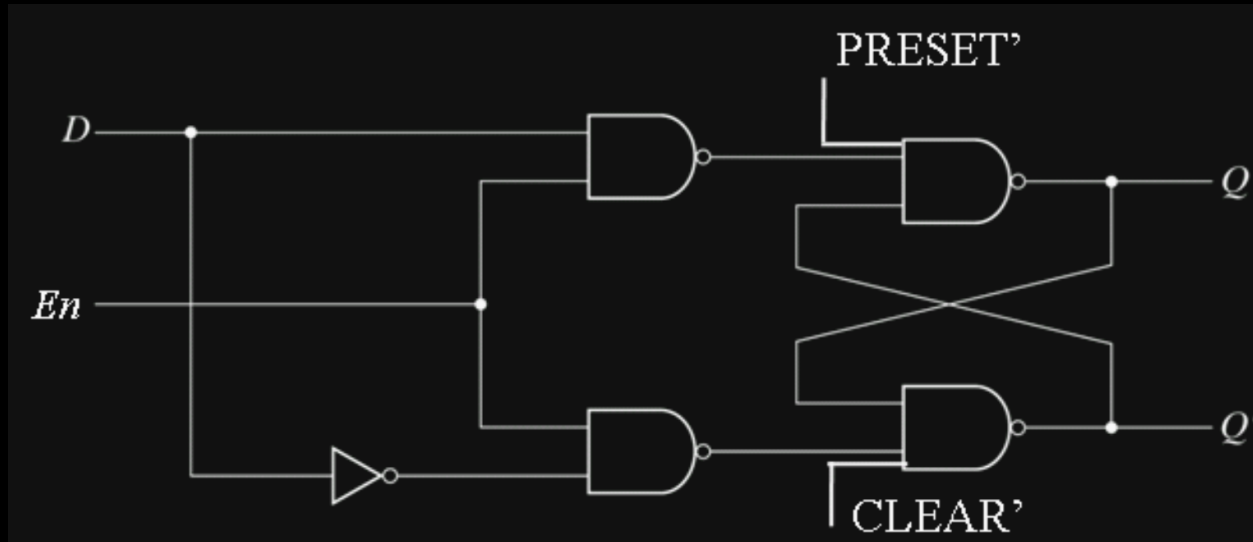
Set

$D = 0$ makes $S = 0$ and $R = 1$

$D = 1$ makes $S = 1$ and $R = 0$

Latches

D Latch with Asynchronous PRESET and CLEAR

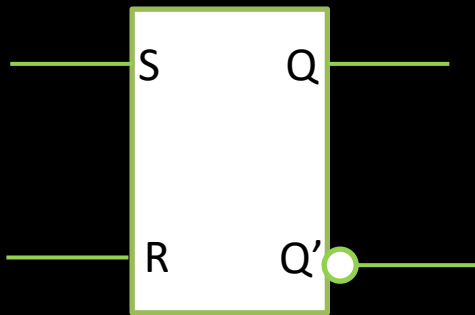


Activating $PRESET'$ (i.e. 0) makes $Q=1$. This in turn maintains $Q'=0$

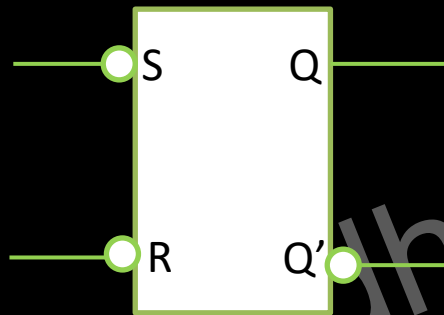
Activating $CLEAR'$ (i.e. 0) makes $Q'=1$. This in turn maintains $Q=0$

Latches

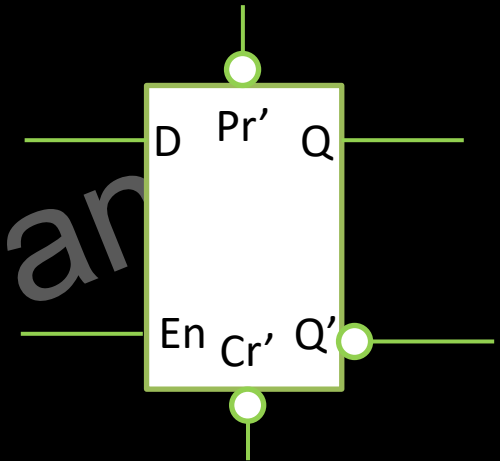
Graphic Symbols



SR Latch



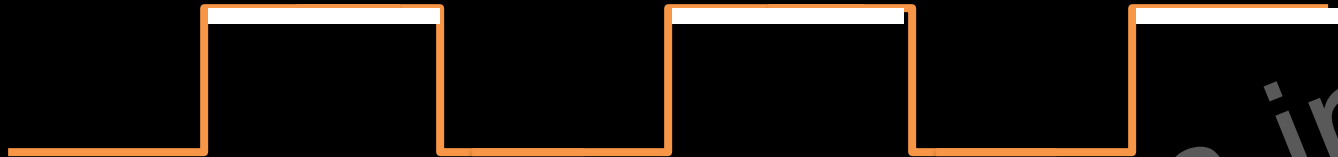
S'R' Latch



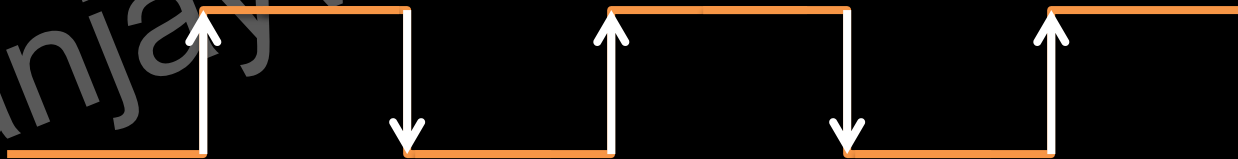
D Latch

Sequential Circuits

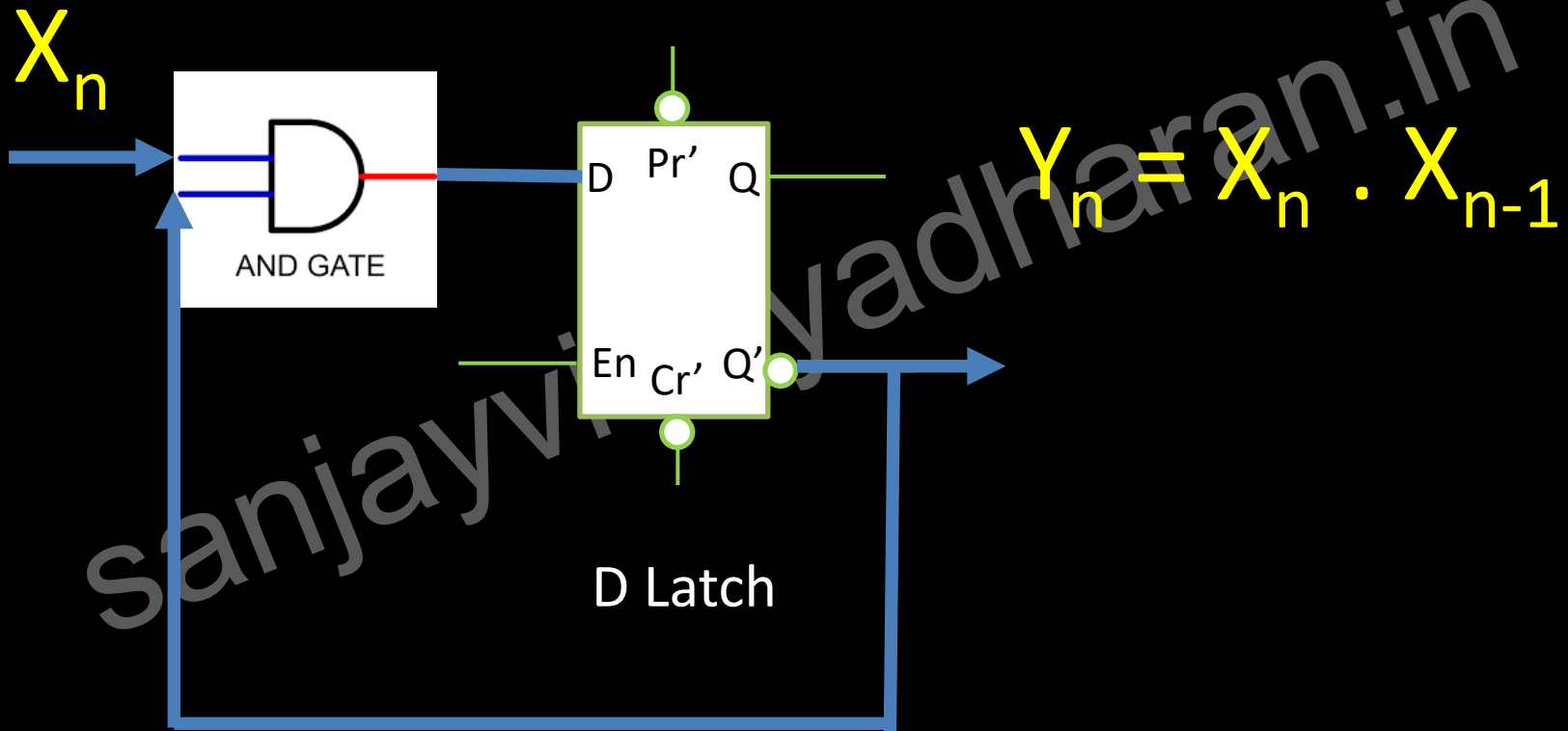
Latch – Responds to change in level of clock pulse



The key to the proper operation of a flip flop is to trigger it only during signal transition.



Race around in Latches



Flip-Flops

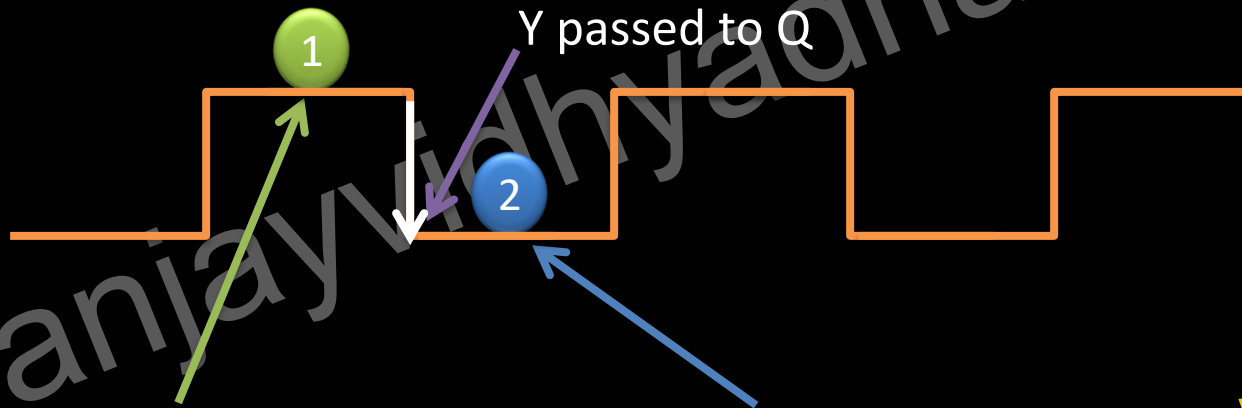
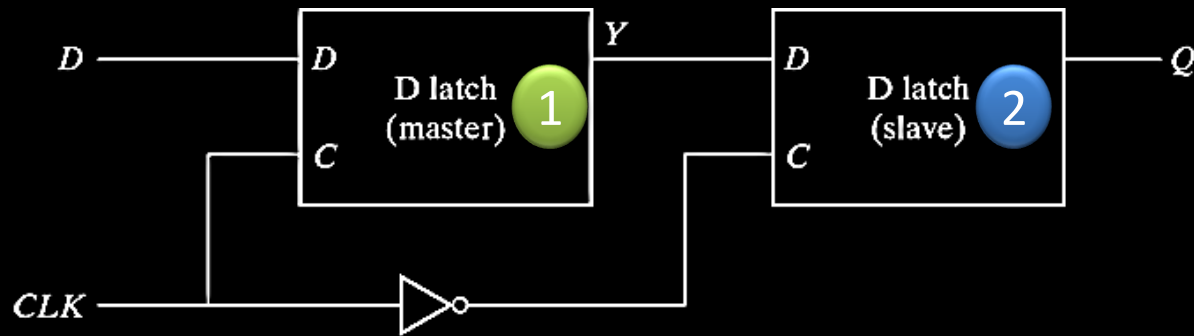
Two ways to build a flip flop

Special configuration of two latches to isolate the output of flip-flop

Gate based design which triggers only during signal transition of clock and is disabled during rest of clock pulse

Edge Triggered D Flip-Flops

Master Slave Flip-flop



If D changes

Y will be affected and not Q

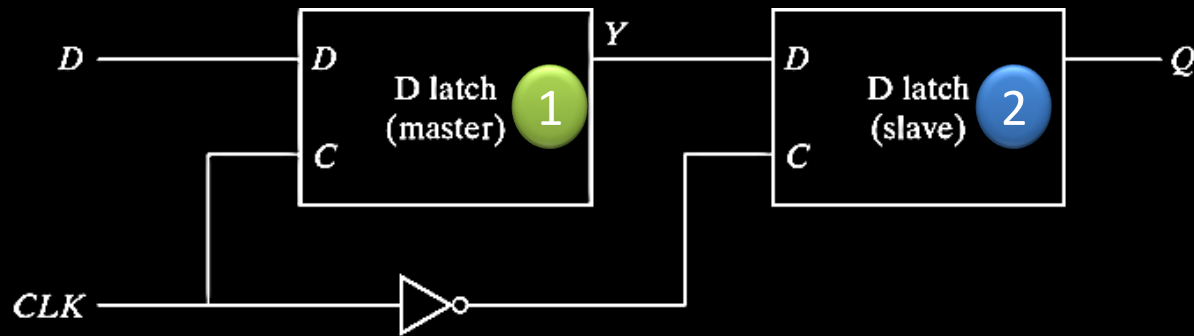
If D changes

Y remains unaffected and Q stable

-ve Edge Triggered

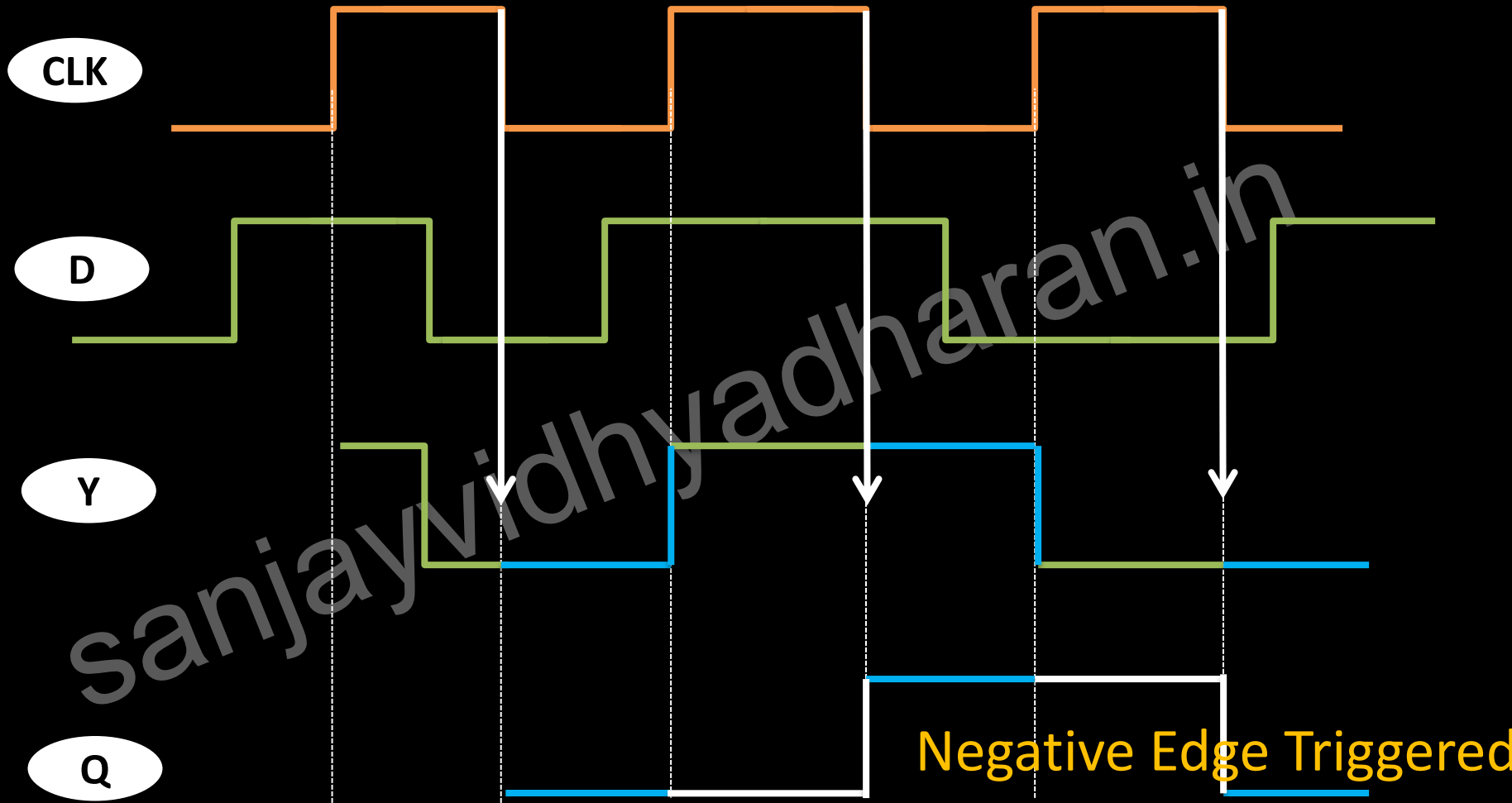
Edge Triggered D Flip-Flops

Master Slave Flip-flop



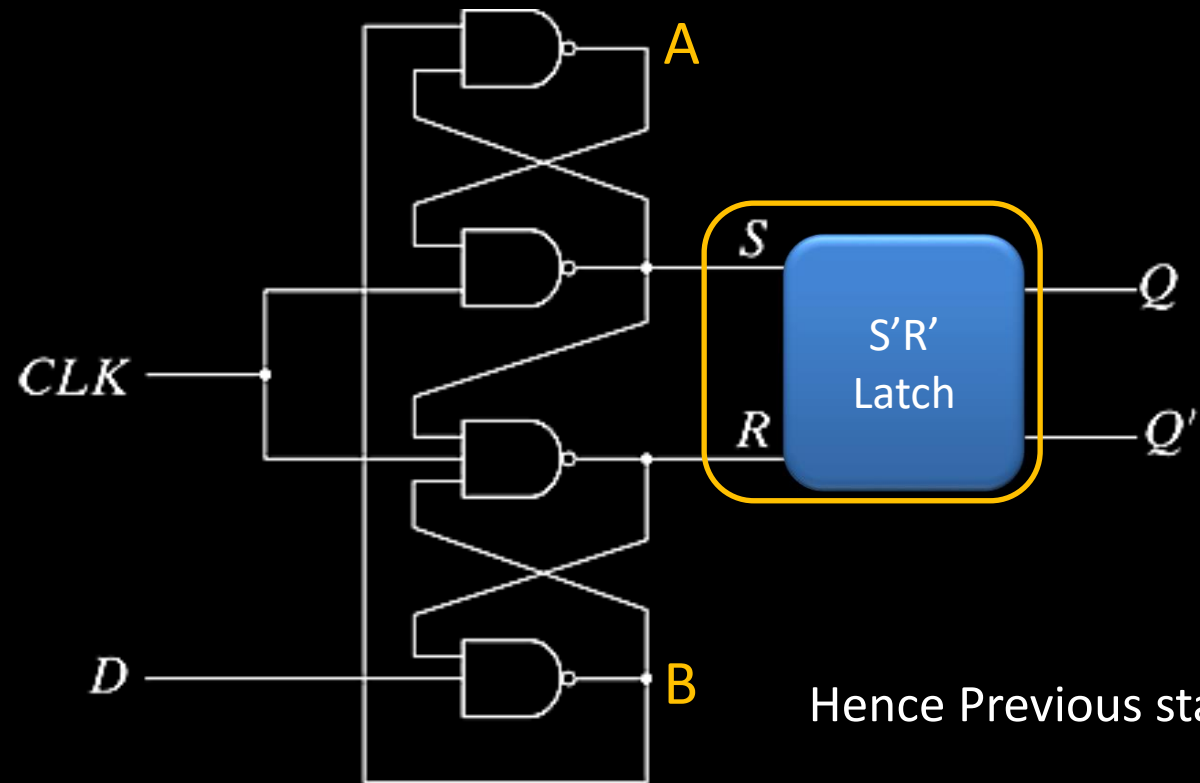
Edge Triggered D Flip-Flops

Master Slave Flip-flop



Edge Triggered D Flip-Flops

D-type positive edge triggered



Case I:

CLK = 0

CLK = 0 $\Rightarrow$ S=1, R=1

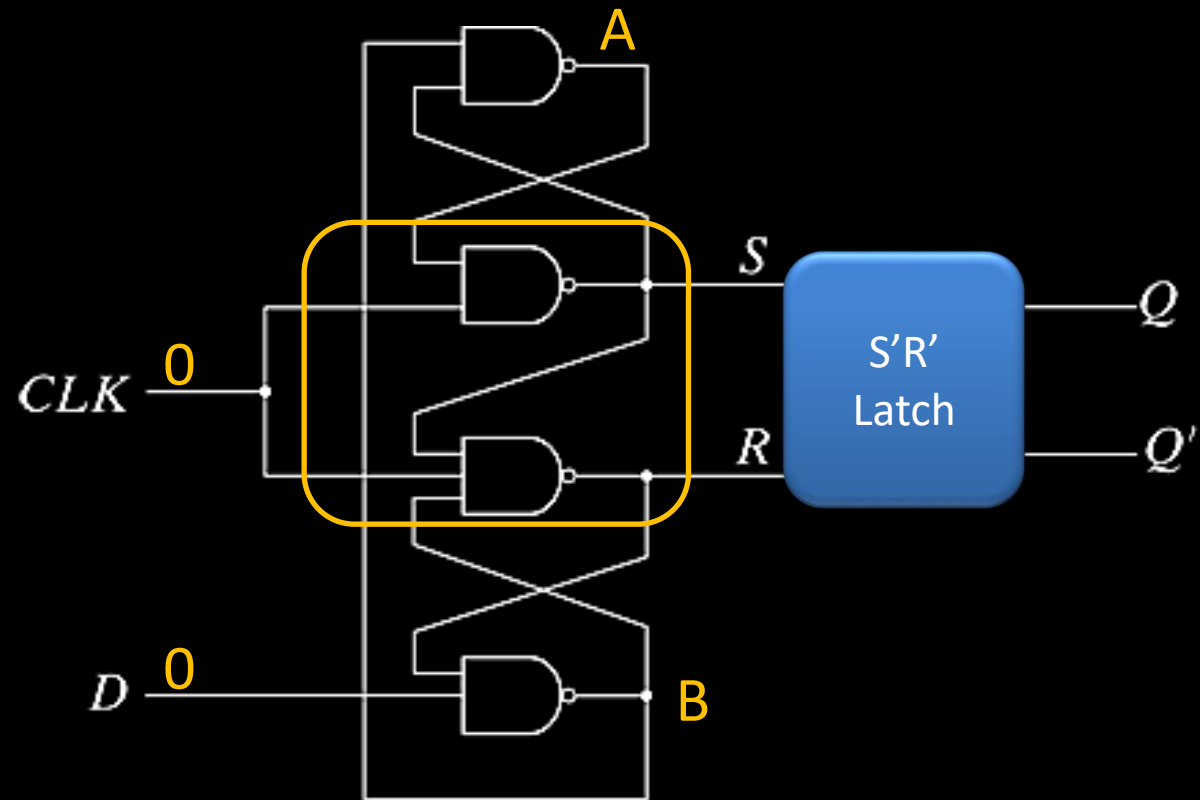
D = 0 $\rightarrow$ 1 $\rightarrow$ 0

S = 1, R = 1 for S'R' latch

Hence Previous state of Q and Q' is maintained

Edge Triggered D Flip-Flops

D-type positive edge triggered



Case 2:

CLK = 1 , D=0, S=1, R=0

B=1, A=0

D -> 0 -> 1 -> 0

B =1 Since R=0

Case 3:

CLK = 1 , D=1, S=0, R=1

B=0, A=1

D -> 1 -> 0 -> 0

B -> 0 -> 1 -> 0

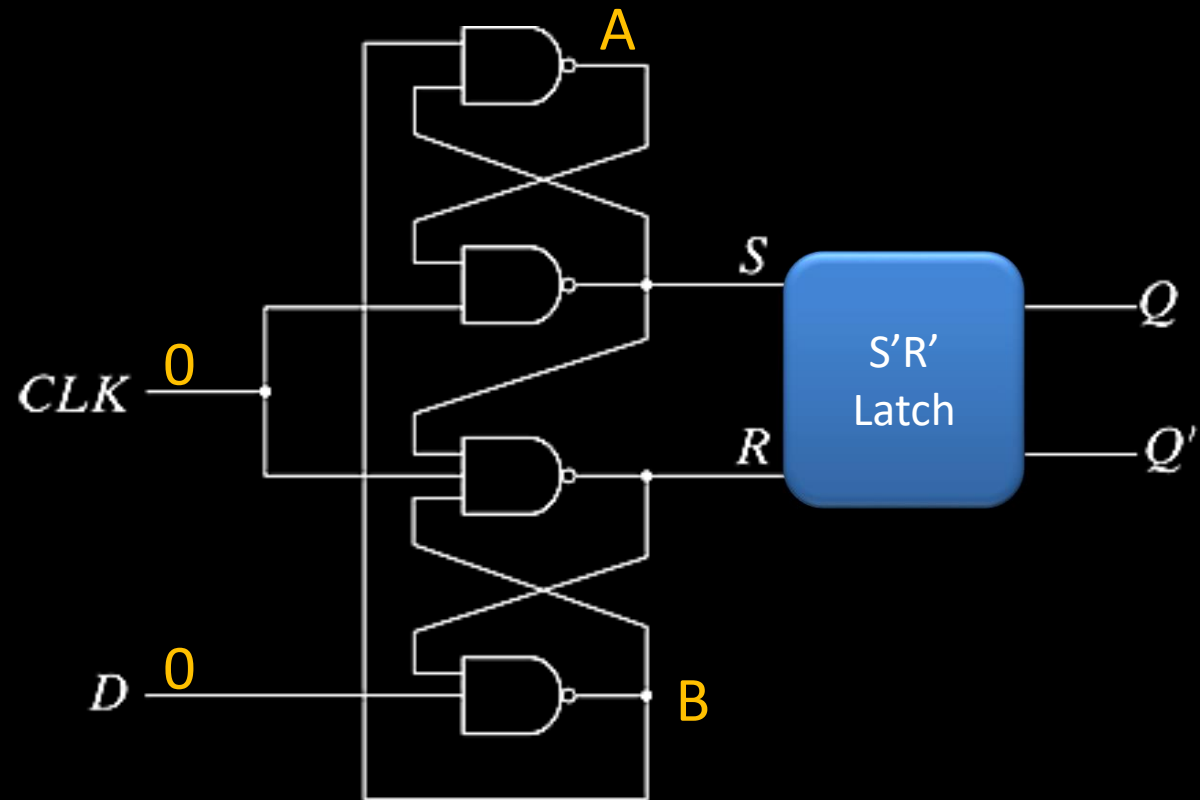
R=1 Since S=0

A=1 Since S=0

Hence Initial state of Q and Q' is maintained

Edge Triggered D Flip-Flops

D-type positive edge triggered



Case 4:

$CLK = 0$, $D=0$, $S=1$, $R=0$

$B=1$, $A=1$, $Q=0$

$D \rightarrow 1$

$B=0$

$CLK \rightarrow 1$

$R=1$

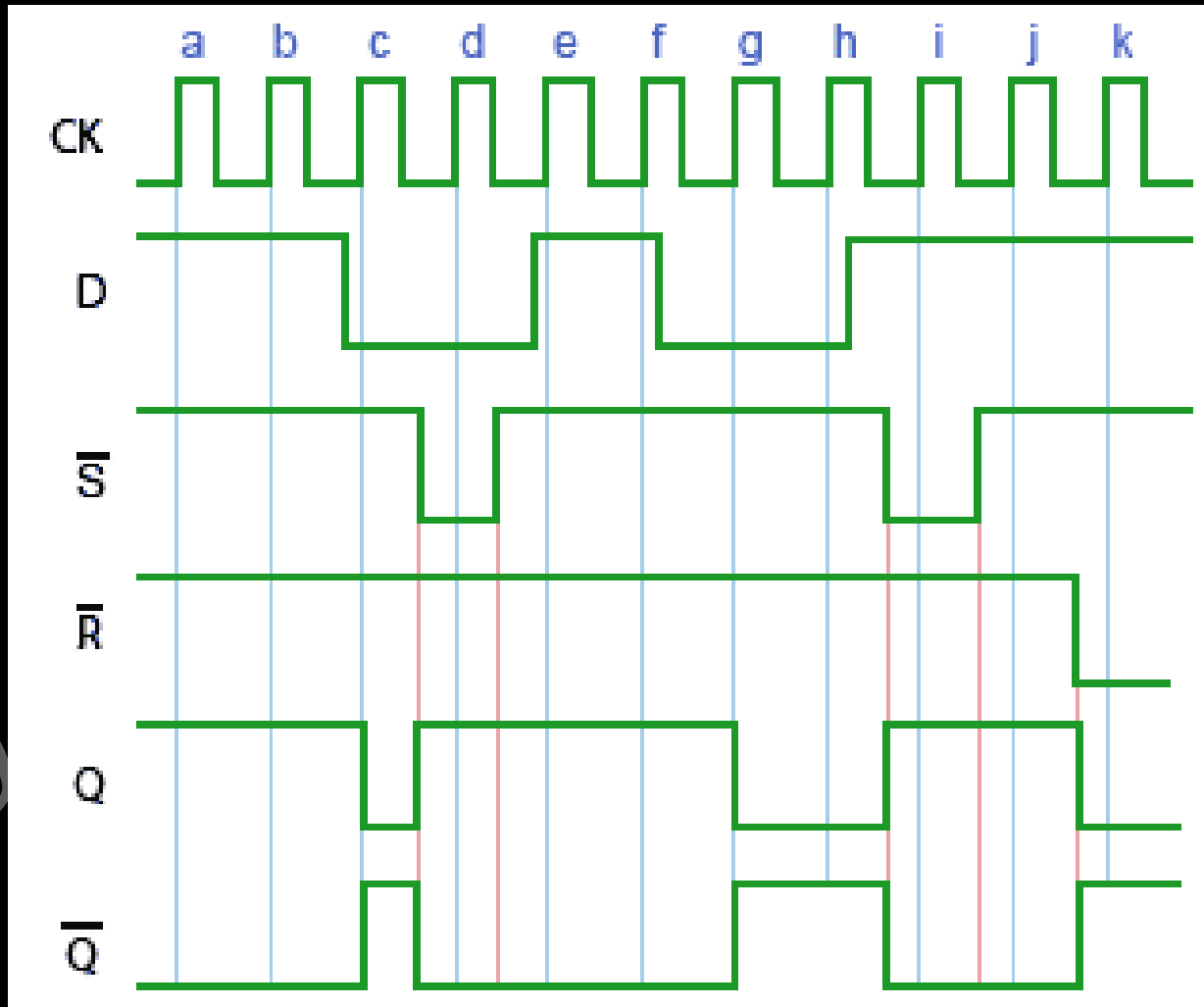
$A=1$

$S=0$

$Q=1$

Edge Triggered D Flip-Flops

D-type positive edge triggered



Thank You

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