Digital Design

Lecture 14: Multiplexers and Demultiplexers

Multiplexers

Multiplexer - combinational circuit that selects binary information from one of many input lines and directs it to single output line

The selection is controlled by Select lines

Normally 2^n input lines, n selection lines and 1 output line

Also called Data Selector

Multiplexers

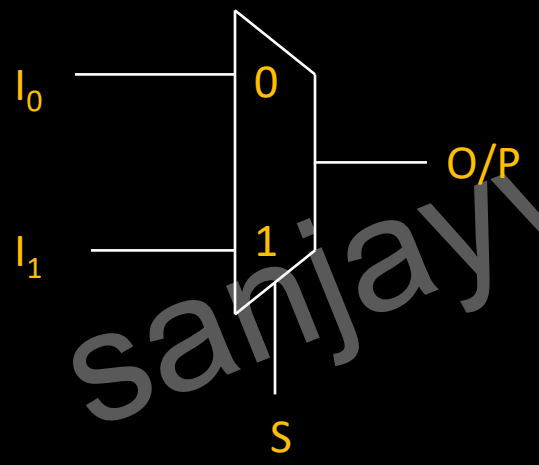
2:1 Multiplexer – 2:1 MUX

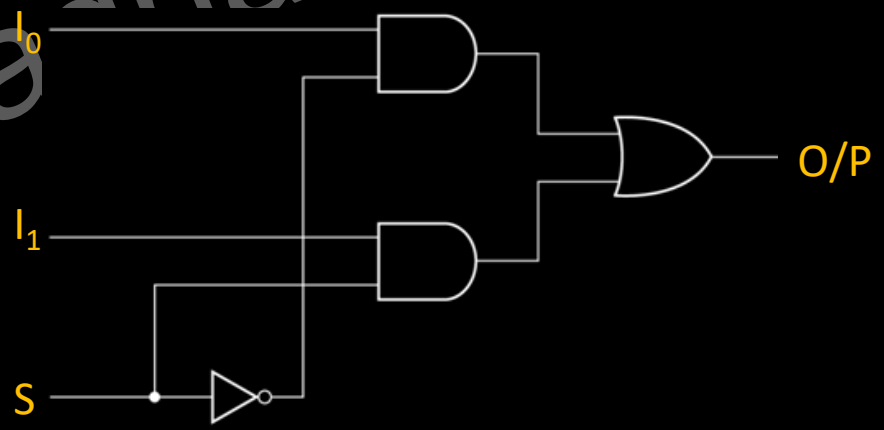
I_0 and I_1 are input lines and S is select line

If s=0 then o/p = I_0

s=1 then o/p = I_1

o/p = $I_0.S' + I_1.S$

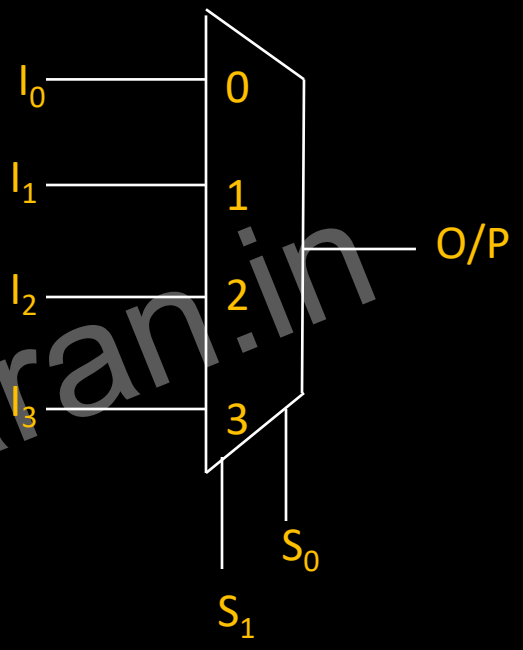




Multiplexers

4:1 Multiplexer – 4:1 MUX

S_1	S_0	O/P
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



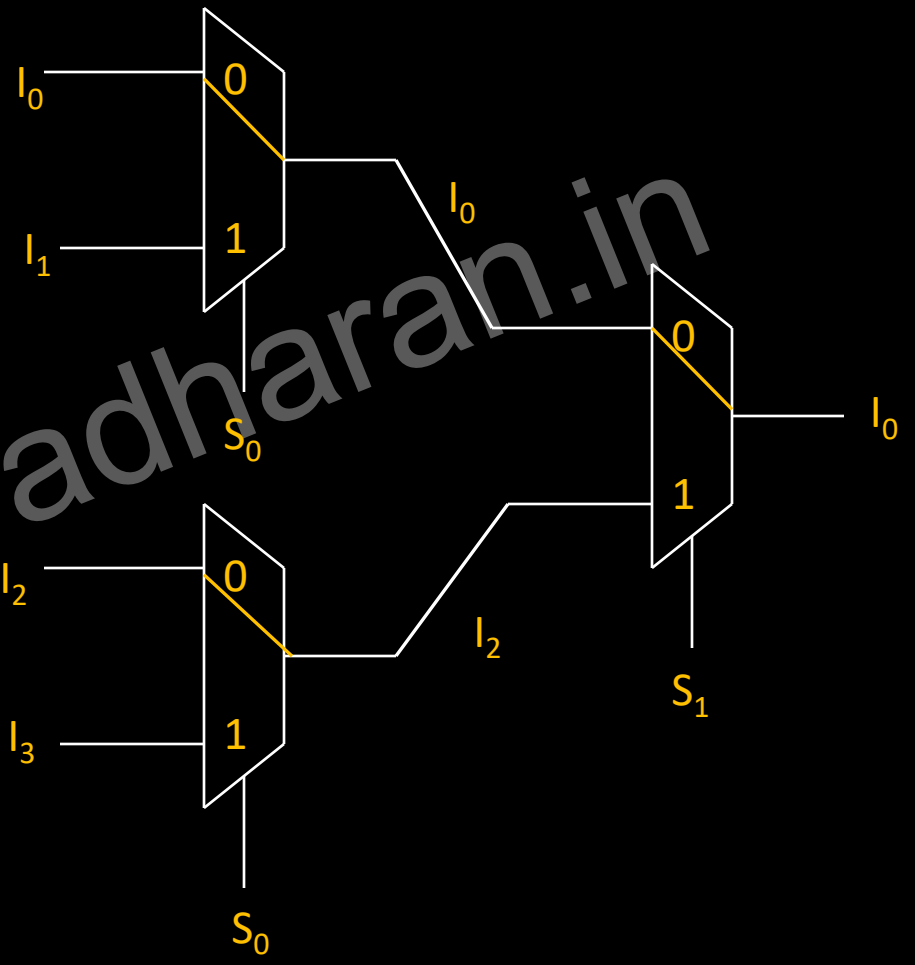
$O/P = S_1'S_0'I_0 + S_1'S_0I_1 + S_1S_0'I_2 + S_1S_0I_3$

Direct Implementation

Multiplexers

4:1 Multiplexer – 4:1 MUX Using 2:1 MUX

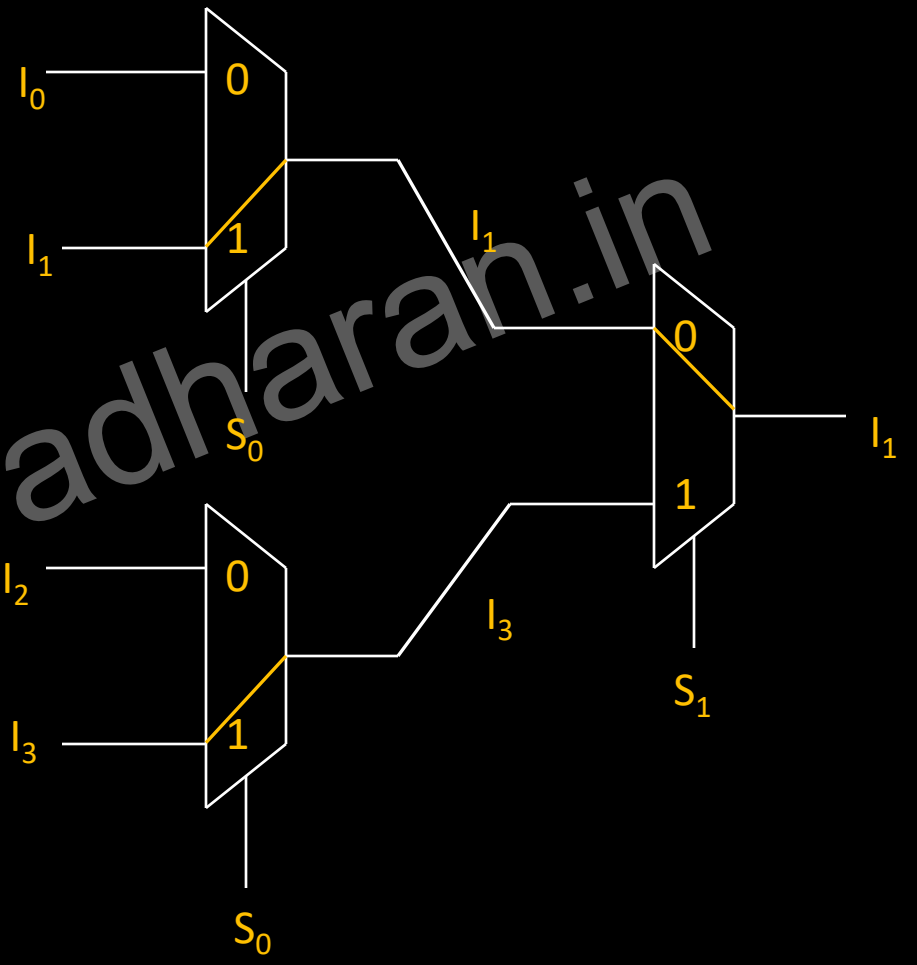
S_1	S_0	O/P
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



Multiplexers

4:1 Multiplexer – 4:1 MUX Using 2:1 MUX

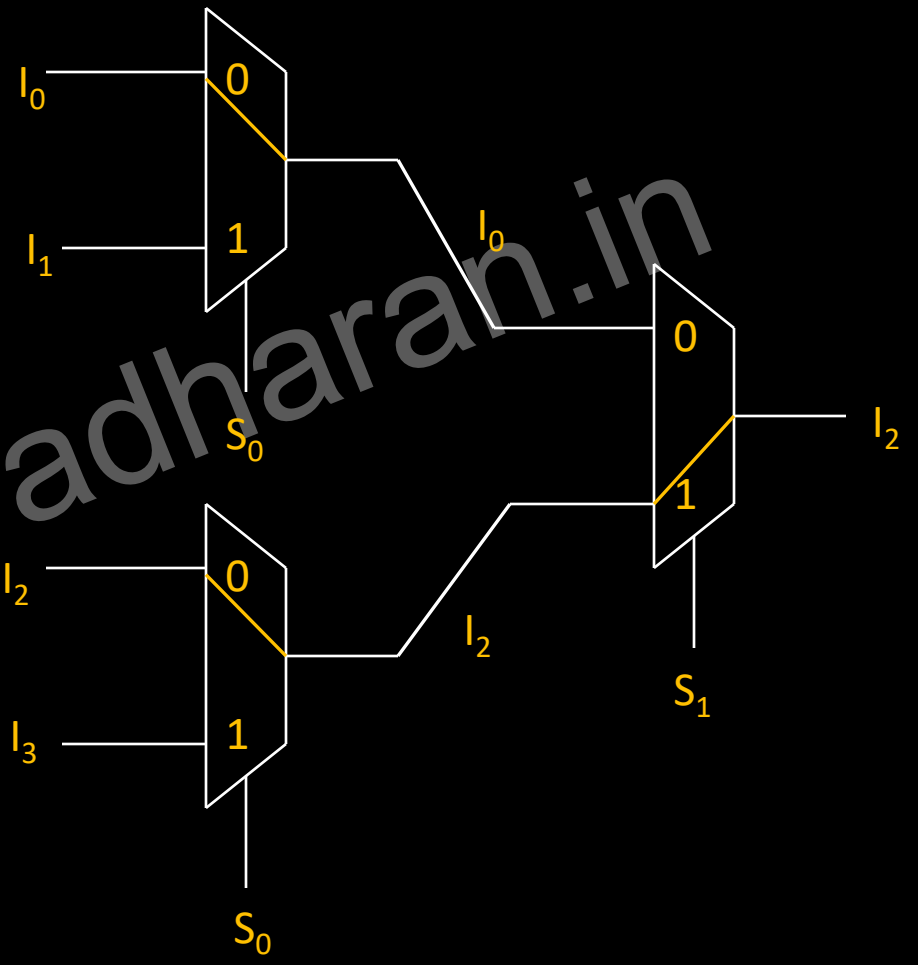
S_1	S_0	O/P
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



Multiplexers

4:1 Multiplexer – 4:1 MUX Using 2:1 MUX

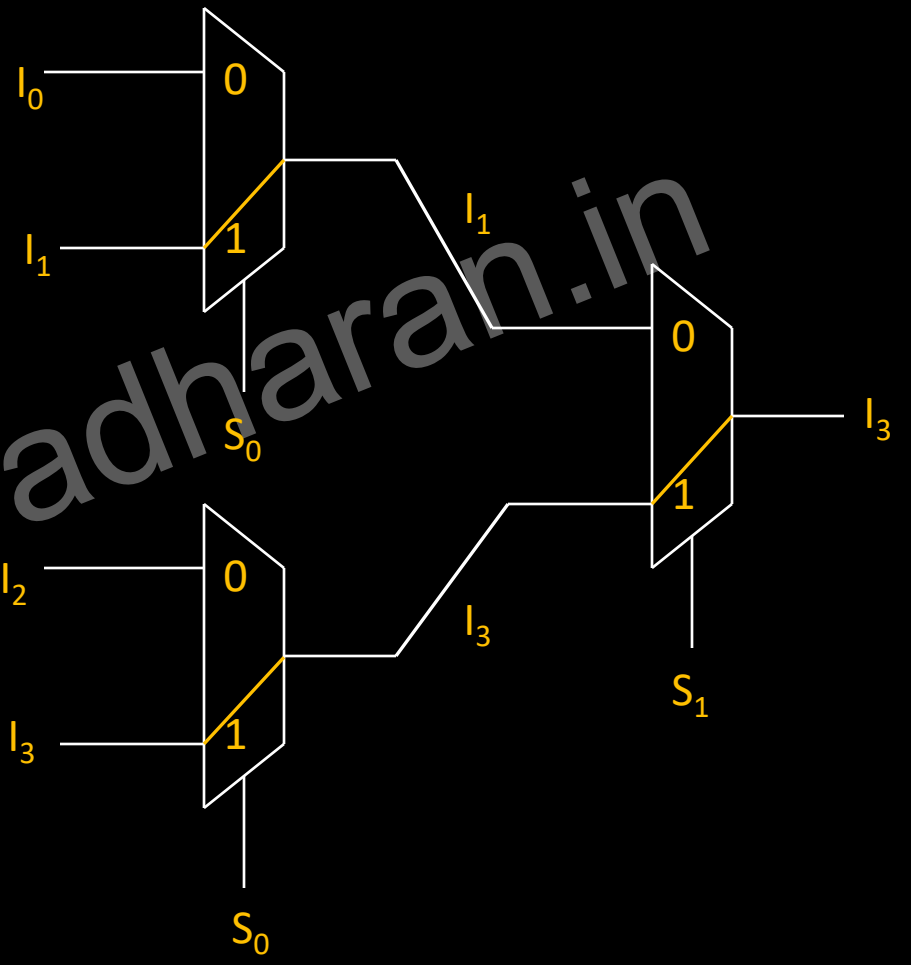
S_1	S_0	O/P
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



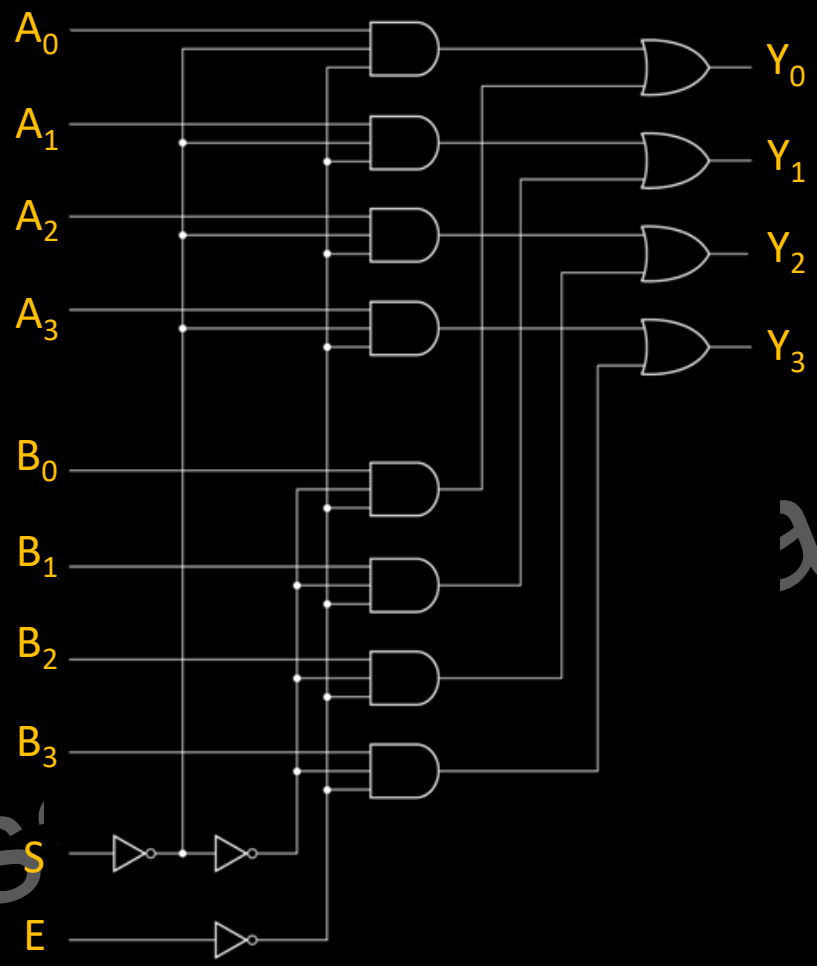
Multiplexers

4:1 Multiplexer – 4:1 MUX Using 2:1 MUX

S_1	S_0	O/P
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



Multiplexers



Multiple Bit Selection Logic

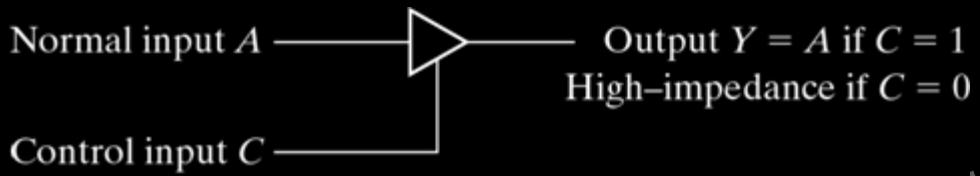
E	S	Output Y
1	0	
1	1	
0	0	
0	1	

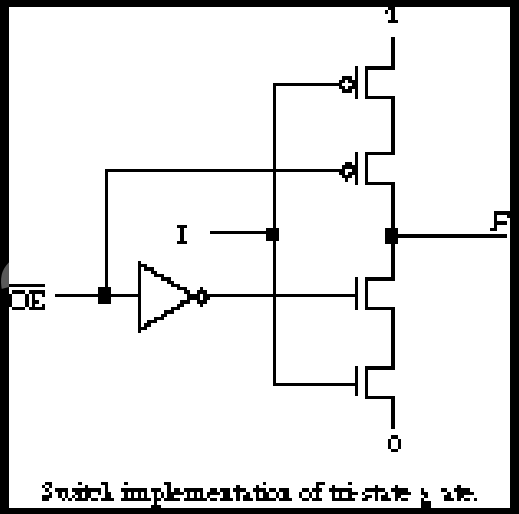
Analyze and Complete the table

Multiplexers

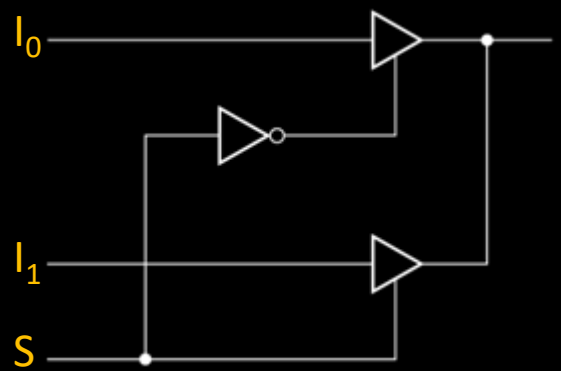
Multiplexers can be constructed using 3-state gates

Tri State Buffer



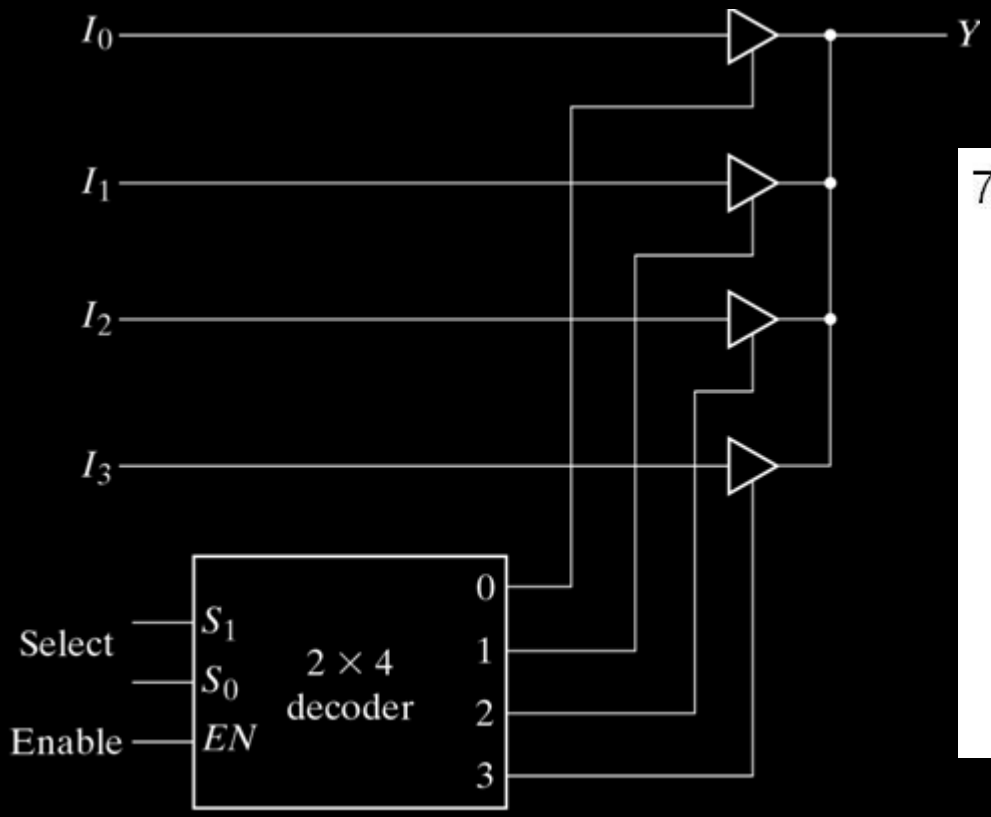


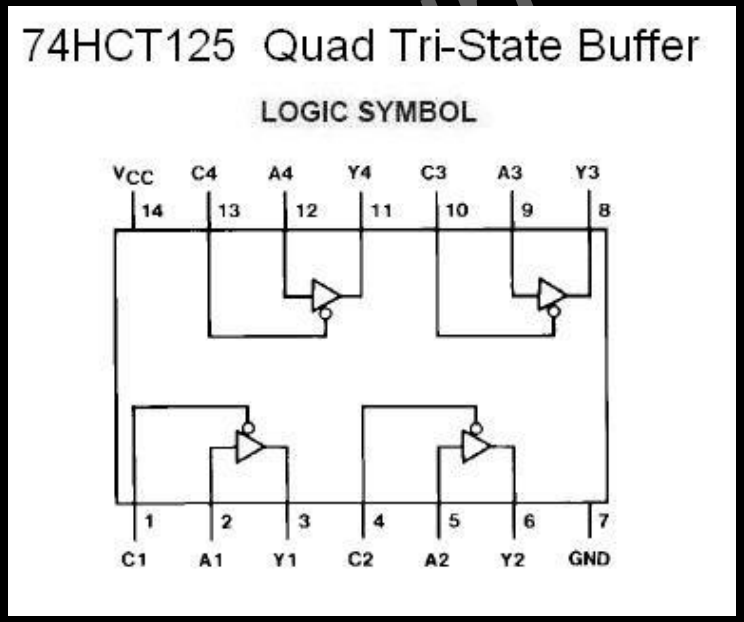
2:1 MUX using Tri-state buffer



Multiplexers

4:1 MUX using Tri-state buffers and 2 to 4 Decoder



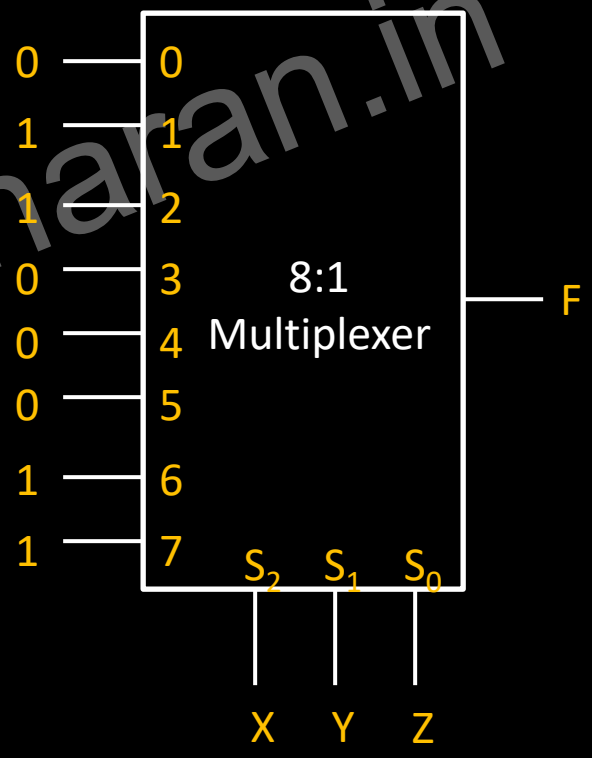


Multiplexers

Boolean Function implementation

$F(X,Y,Z) = \sum (1, 2, 6, 7)$

X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



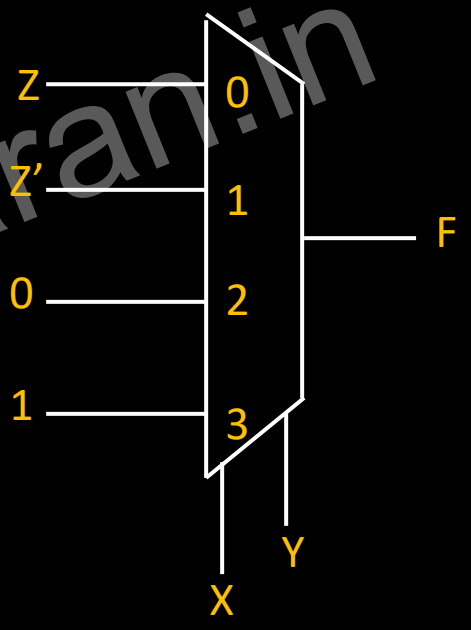
Multiplexers

Boolean Function implementation

$F(X,Y,Z) = \sum (1, 2, 6, 7)$

X	Y	Z	F	
0	0	0	0	F = Z
0	0	1	1	
0	1	0	1	F = Z’
0	1	1	0	
1	0	0	0	F = 0
1	0	1	0	
1	1	0	1	F = 1
1	1	1	1	

4:1 Multiplexer



Multiplexers

Boolean Function implementation

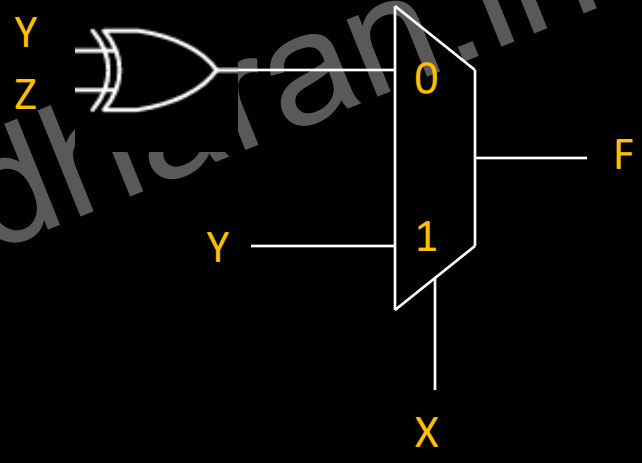
$F(X,Y,Z) = \sum (1, 2, 6, 7)$

X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

$F = Y \oplus Z$

$F = Y$

2:1 Multiplexer



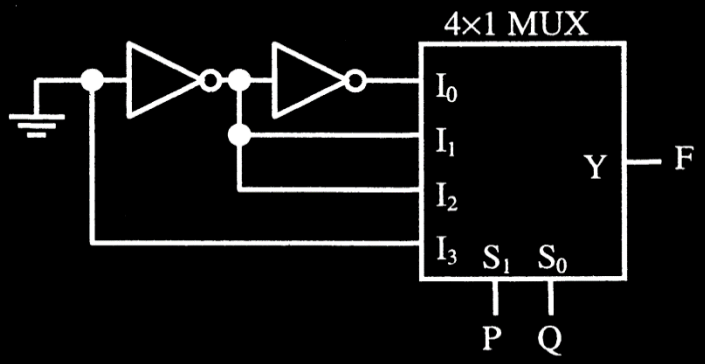
Multiplexers

Boolean Function implementation

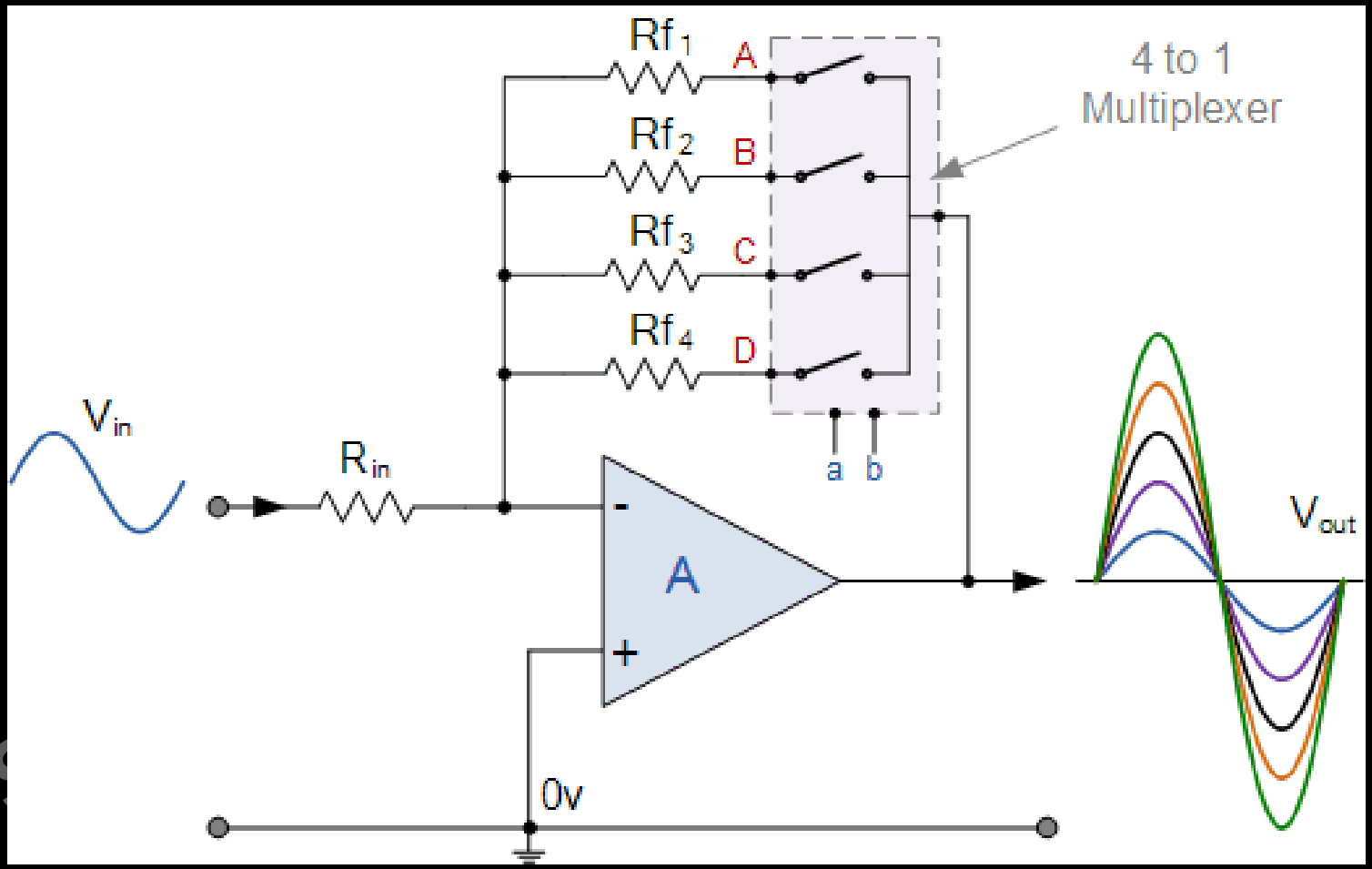
1. F (X,Y,Z) = ∑ (1, 3, 5, 6, 7) using 4:1 MUX and 2:1 MUX

2. F (A, B, C, D) = ∑ (1, 3, 4, 11, 12, 13, 14, 15) Using 8:1 MUX and 4:1 MUX

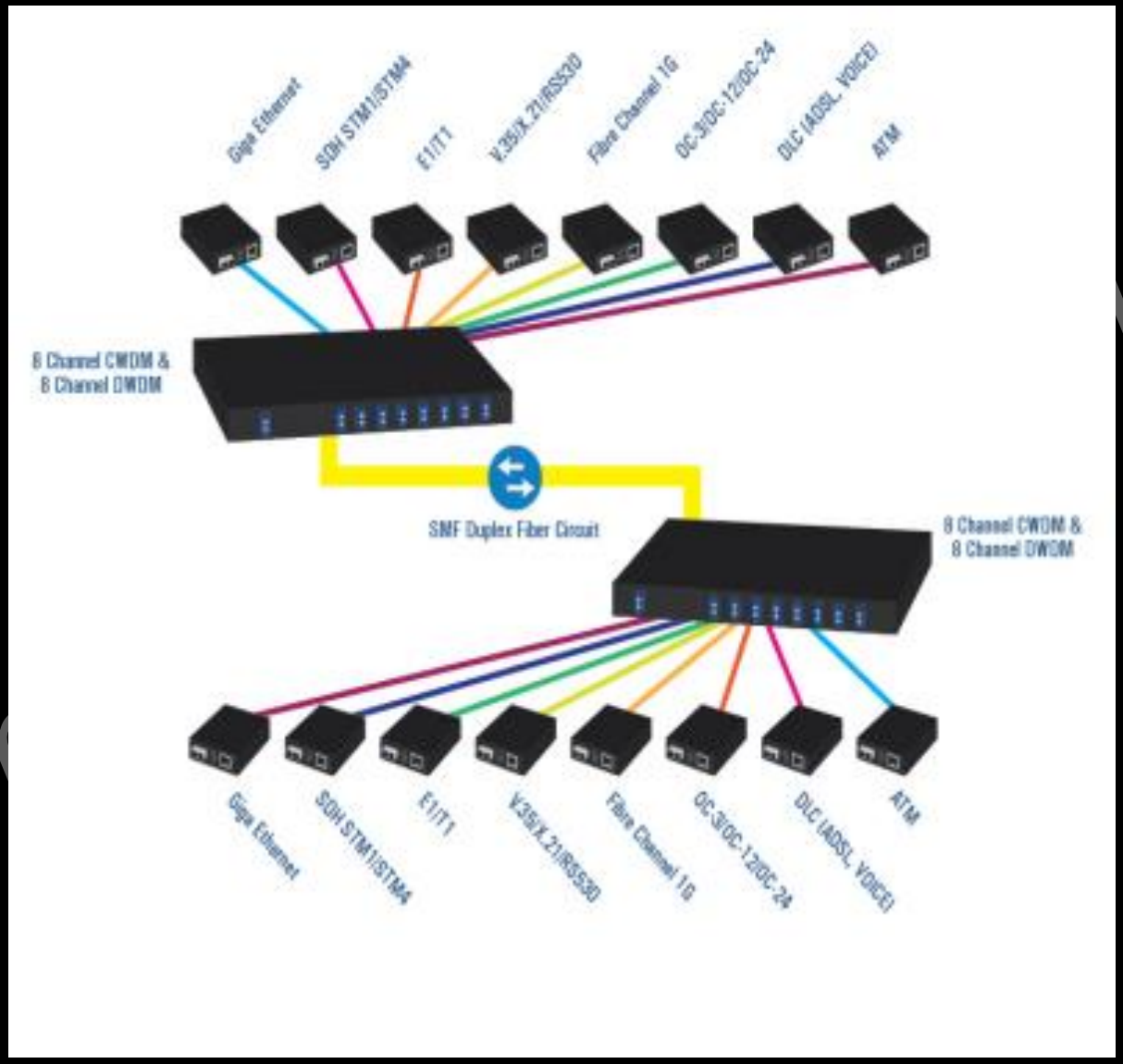
3. The logic function implemented by the circuit below is (Ground implies logic '0')



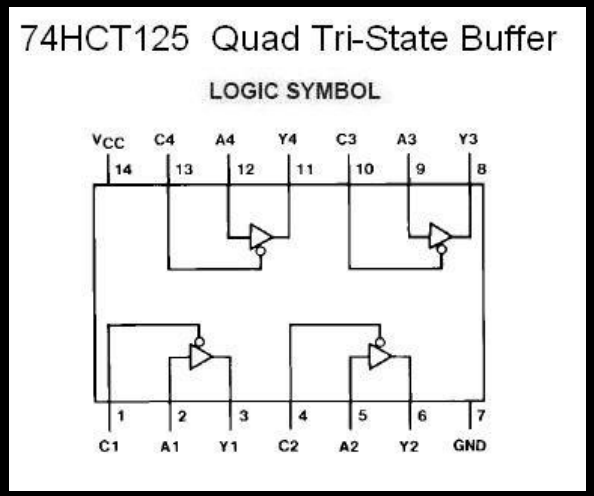
Multiplexers



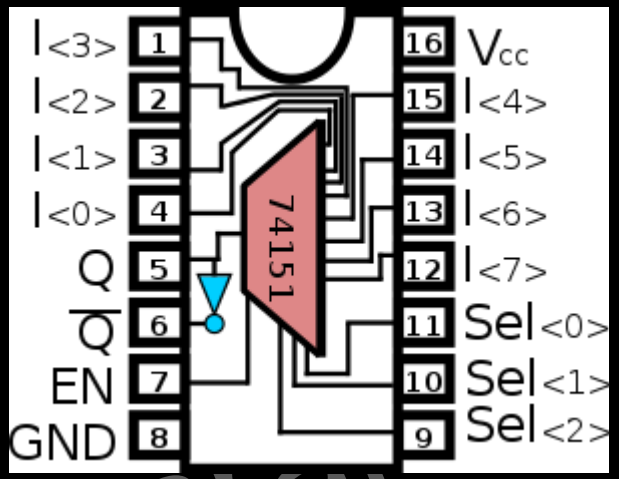
Multiplexers



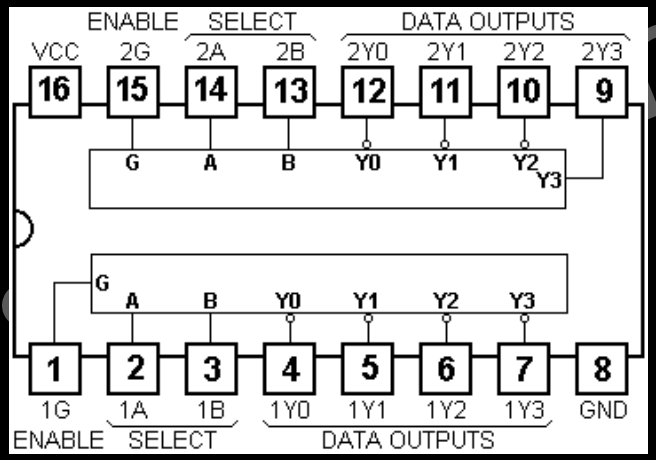
74XX series ICs



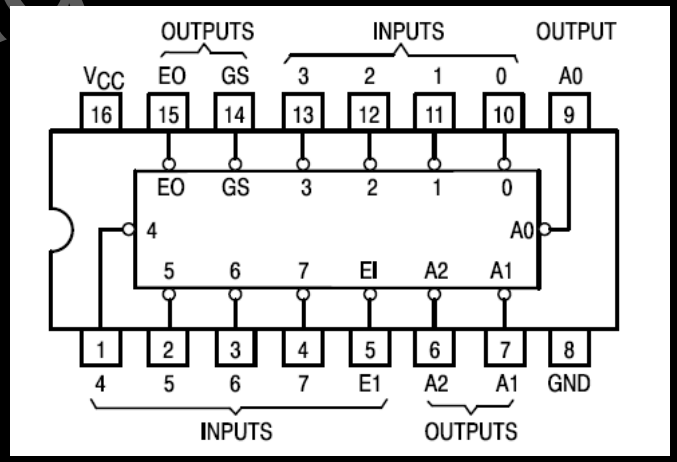
Tristate Buffer



Mux



Decoder



Enecoder

Thank You