



**BITS Pilani**

Hyderabad Campus

Department of Electrical Engineering

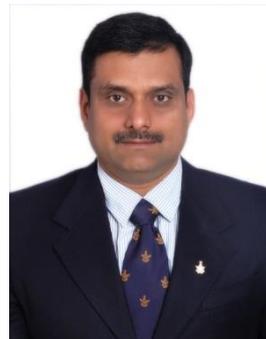


**Digital Design : 2020-21**

**Lab 8**

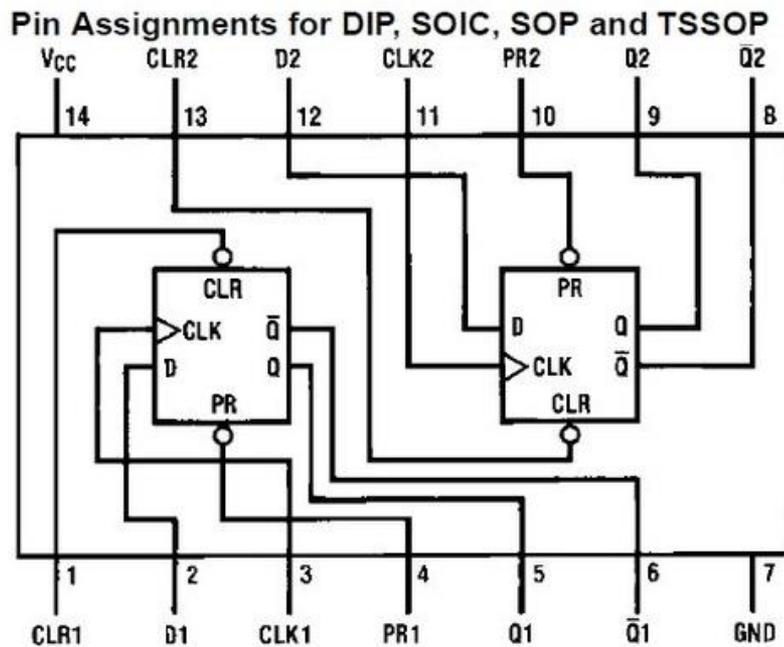
**Sequential Circuit Design using  
D and JK Flipflops**

**By Dr. Sanjay Vidhyadharan**



# The 74HCT74 D Flipflop

## Connection Diagram



## Truth Table

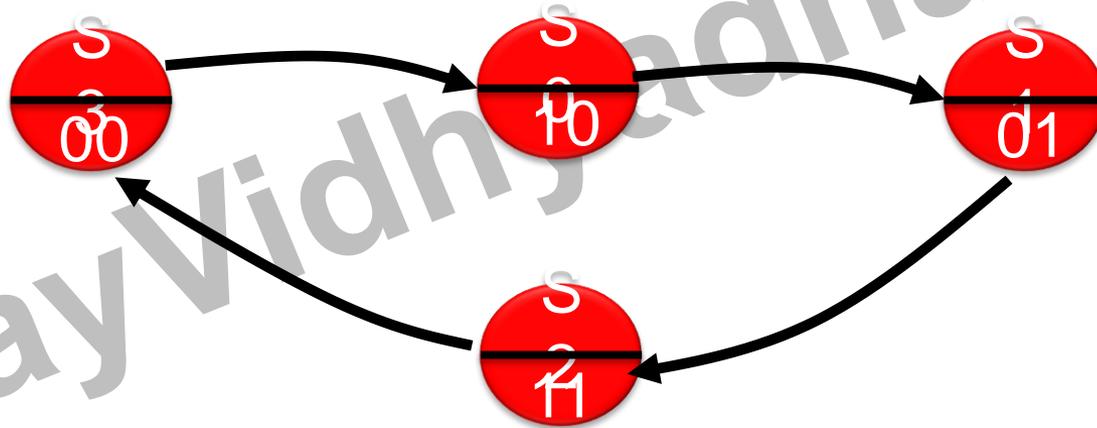
Inputs				Outputs	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	$\uparrow$	H	H	L
H	H	$\uparrow$	L	L	H
H	H	L	X	Q0	$\bar{Q}0$

**Note:** Q0 = the level of Q before the indicated input conditions were established.

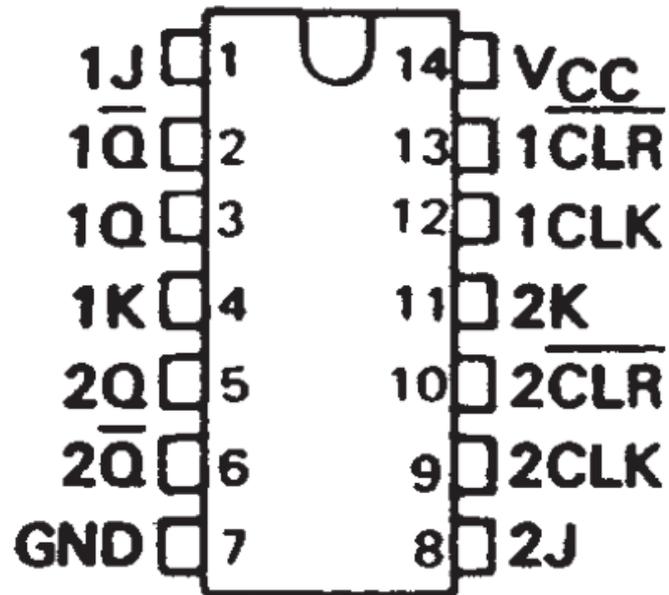
**Note 1:** This configuration is nonstable; that is, it will not persist when pre-set and clear inputs return to their inactive (HIGH) level.

# The 74HCT74 D Flipflop

Problem 1: Design a Counter using D-Flipflop as per state diagram given below:-



# The 74HCT107 JK Flipflop

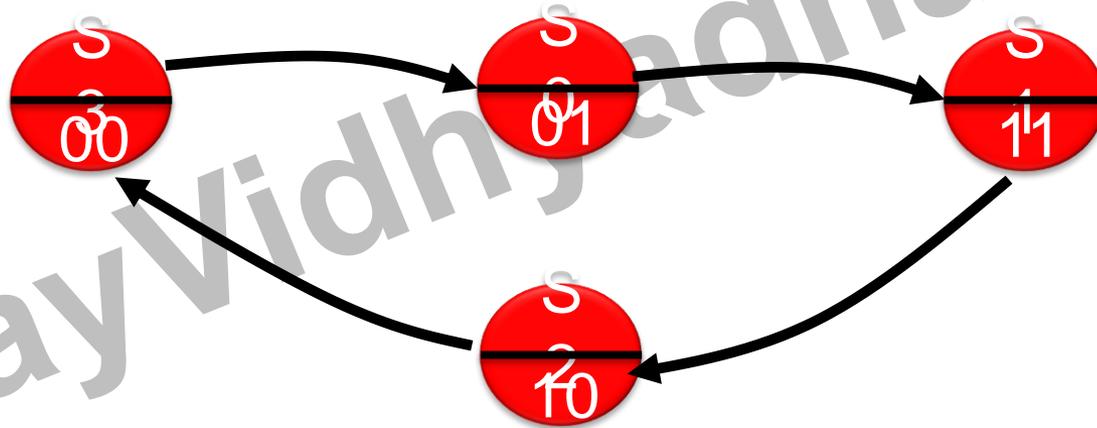


'LS107A  
FUNCTION TABLE

INPUTS				OUTPUTS	
$\bar{CLR}$	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	$Q_0$	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	TOGGLE
H	H	X	X	$Q_0$	$\bar{Q}_0$

# The 74HCT74 D Flipflop

Problem 1: Design a Gray Counter using JK-Flipflop as per state diagram given below:-





# Demonstration