

Digital Design: 2020-21 Parity Generator & By Dr. Sanjay Vidhyadharan

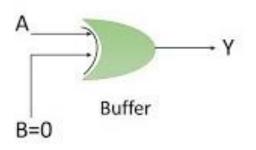
3-	bit Messa	ge	Odd		
х	Y	z	Parity Bit	aran.in	
0	0	0	1	43	
0	0	1	0		
0	1	0	0		
0	1	1	1		
1	0	0	0		
1	0	1	1		
1	1	0	1		
1	1	1	0		

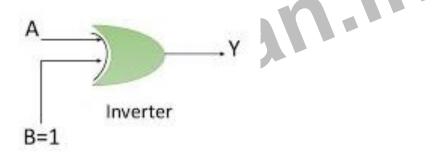


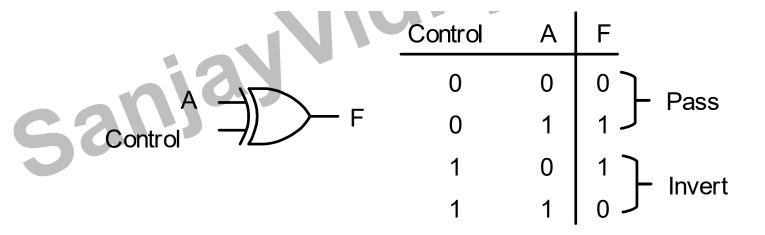
3-bit Message			Even	
х	Y	z	Parity Bit	ni
0	0	0	0	LSU.
0	0	1	1	
0	1	0	1	
0	1	1	0	
1	0	0	1	
1	0	1	0	
1	1	0	0	
1	1	1	1	

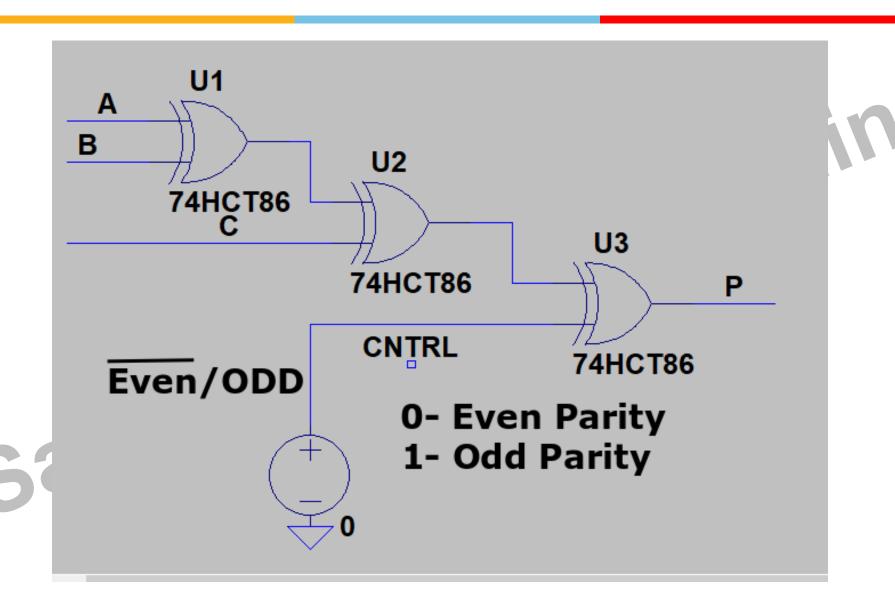


EX-OR Gate As Buffer and Inverter









Binary to Gray Converter

Problem 1:Binary to Gray Converter

De	ecimal Number	4 bit Binary Number ABCD	4 bit Gray Code G ₁ G ₂ G ₃ G ₄		1
	0	0000	0000	B ₃ — G ₃	
	2 3 4	0 0 1 0 0 0 1 1 0 1 0 0	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	B_2 $X2$ G_2	
	5 6 7	0 1 0 1 0 1 1 0 0 1 1 1	0 1 1 1 0 1 0 1 0 1 0 0	B_1 $X1$ G_1	
	8 9 10	1000 1001 1010	1 1 0 0 1 1 0 1 1 1 1 1		
	11 12 13	1011 1100 1101	1 1 1 0 1 0 1 0 1 0 1 1	B_0 X_0	
	14 15	1110	1001		



Half Adder

Problem 2: Half Adder

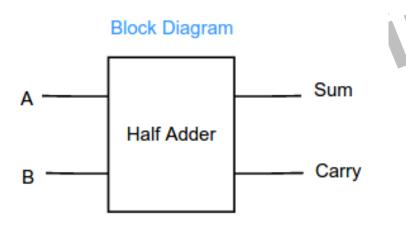
Truth Table

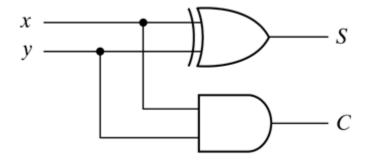
Inp	out	Output		
Α	В	Sum	Carry	
0	0	0	0	
0	1	1	0	
1	0	1	0	
1	1	0	1	

$$Sum(S) = x \oplus y$$

$$Carry(C) = xy$$

$$Carry(C) = xy$$

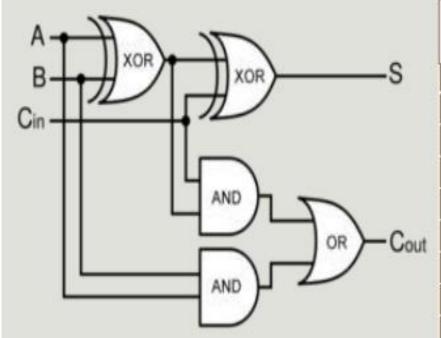






Full Adder

Problem 3: Full Adder



INF	TU	CARRY IN	OUTPUT		
x	y	C in	C _{out}	s	
0	0	0	0	0	
0	0	1	0	1	
0	1	0	0	1	
0	1	1	1	0	
1	0	0	0	1	
1	0	1	1	0	
1	1	0	1	0	
1	1	1	1	1	



FULL ADDER CIRCUIT & TRUTH TABLE

Demonstration Sanial