# Digital Design
# First Semester 2020-21
# Tutorial : 09

# Sequence Detector

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1. Design a 11011 sequence detector using JK flip-flops. Allow overlap.

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Step 1

We are designing a sequence detector for a 5-bit sequence, so we need 5 states. We label these states A, B, C, D, and E. State A is the initial state.

Step 2

Characterize Each State by What has been Input and What is Expected State

| State | Has | Awaiting |
|---|---|---|
| A | -- | 11011 |
| B | 1 | 1011 |
| C | 11 | 011 |
| D | 110 | 11 |
| E | 1101 | 1 |

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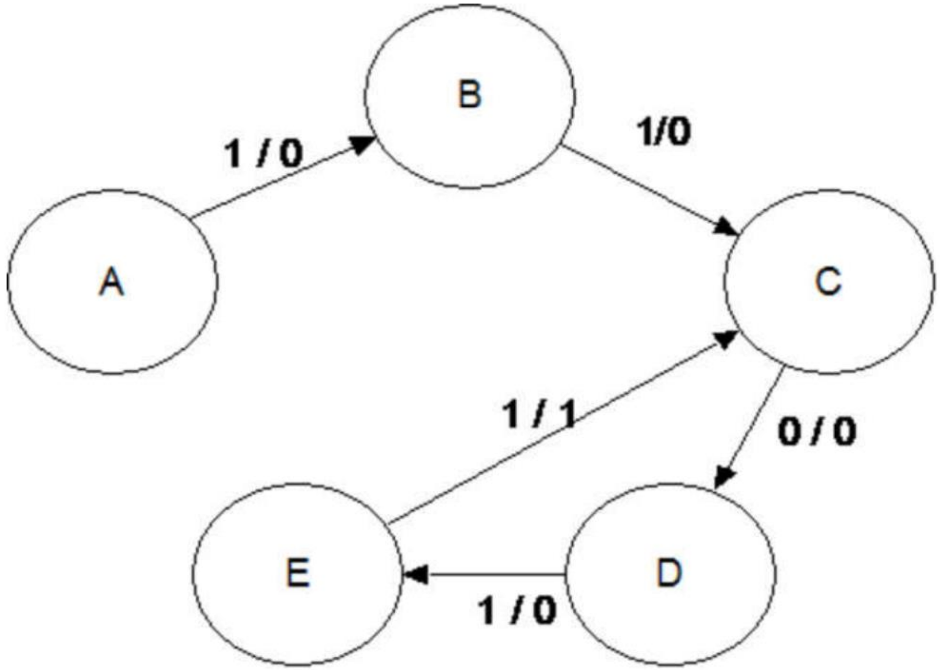
Step 3
Do the Transitions for the Expected Sequence



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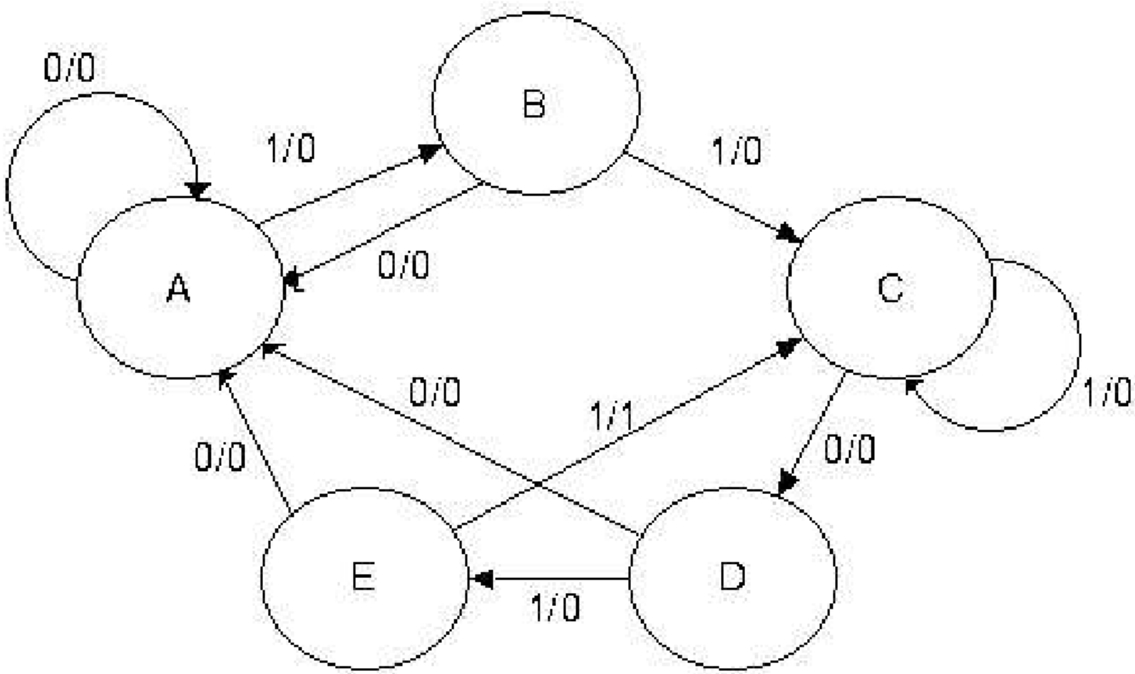
Step 4 Complete the State Diagram



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Step 5 Make State Table

| Present State | Next State / Output | |
|---|---|---|
| | X = 0 | X = 1 |
| A | A / 0 | B / 0 |
| B | A / 0 | C / 0 |
| C | D / 0 | C / 0 |
| D | A / 0 | E / 0 |
| E | A / 0 | C / 1 |

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Step 6 – Determine the Number of Flip-Flops Required
We have 5 states, so N = 5. We solve the equation 2P-1 < 5 £ 2P by inspection, noting that it is solved by P = 3. So we need three flip-flops.

Step 7 – Assign a unique P-bit binary number (state vector) to each state.
The simplest way is to make the following assignments

A = 000
B = 001
C = 011 Note that states 010, 110, and 111 are not used.
D = 100
E = 101

Occasionally, a better assignment can be detected by inspection of the next state table. I note that the next states in the table cluster into two disjoint sets for X = 0 and X = 1. For X = 0 the possible next states are A and D For X = 1 the possible next states are B, C, and E. For this reason, I elect to give even number assignments to states A and D, and to give odd number assignments to states B, C, and E.

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Step 8 – Generate the Transition Table With Output

| Present State | | Next State / Output | |
|---|---|---|---|
| | | X = 0 | X = 1 |
| | $Y_2Y_1Y_0$ | $Y_2Y_1Y_0$ / Z | $Y_2Y_1Y_0$ / Z |
| A | 0 0 0 | 0 0 0 / 0 | 0 0 1 / 0 |
| B | 0 0 1 | 0 0 0 / 0 | 0 1 1 / 0 |
| C | 0 1 1 | 1 0 0 / 0 | 0 1 1 / 0 |
| D | 1 0 0 | 0 0 0 / 0 | 1 0 1 / 0 |
| E | 1 0 1 | 0 0 0 / 0 | 0 1 1 / 1 |

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Step 9 – Separate the Transition Table into Three Tables, One for Each Flip-Flop

| Y2 | | | Y1 | | | Y0 | | |
|---|---|---|---|---|---|---|---|---|
| PS | Next State | | PS | Next State | | PS | Next State | |
| $Y_2Y_1Y_0$ | X = 0 | X = 1 | $Y_2Y_1Y_0$ | X = 0 | X = 1 | $Y_2Y_1Y_0$ | X = 0 | X = 1 |
| 0 0 0 | 0 | 0 | 0 0 0 | 0 | 0 | 0 0 0 | 0 | 1 |
| 0 0 1 | 0 | 0 | 0 0 1 | 0 | 1 | 0 0 1 | 0 | 1 |
| 0 1 1 | 1 | 0 | 0 1 1 | 0 | 1 | 0 1 1 | 0 | 1 |
| 1 0 0 | 0 | 1 | 1 0 0 | 0 | 0 | 1 0 0 | 0 | 1 |
| 1 0 1 | 0 | 0 | 1 0 1 | 0 | 1 | 1 0 1 | 0 | 1 |

Match $Y_1$ $Y_2 \cdot Y_0'$ 0 $Y_0$ 0 1

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Step 10 – Separate the Transition Table into Three Tables, One for Each Flip-Flop

| Y2 | | | Y1 | | | Y0 | | |
|---|---|---|---|---|---|---|---|---|
| PS | Next State | | PS | Next State | | PS | Next State | |
| $Y_2Y_1Y_0$ | X = 0 | X = 1 | $Y_2Y_1Y_0$ | X = 0 | X = 1 | $Y_2Y_1Y_0$ | X = 0 | X = 1 |
| 0 0 0 | 0 | 0 | 0 0 0 | 0 | 0 | 0 0 0 | 0 | 1 |
| 0 0 1 | 0 | 0 | 0 0 1 | 0 | 1 | 0 0 1 | 0 | 1 |
| 0 1 1 | 1 | 0 | 0 1 1 | 0 | 1 | 0 1 1 | 0 | 1 |
| 1 0 0 | 0 | 1 | 1 0 0 | 0 | 0 | 1 0 0 | 0 | 1 |
| 1 0 1 | 0 | 0 | 1 0 1 | 0 | 1 | 1 0 1 | 0 | 1 |
| Match | $Y_1$ | $Y_2 \cdot Y_0'$ | | 0 | $Y_0$ | | 0 | 1 |

D2 = X’·Y1 + X·Y2·Y0’
D1 = X ·Y0
D0 = X

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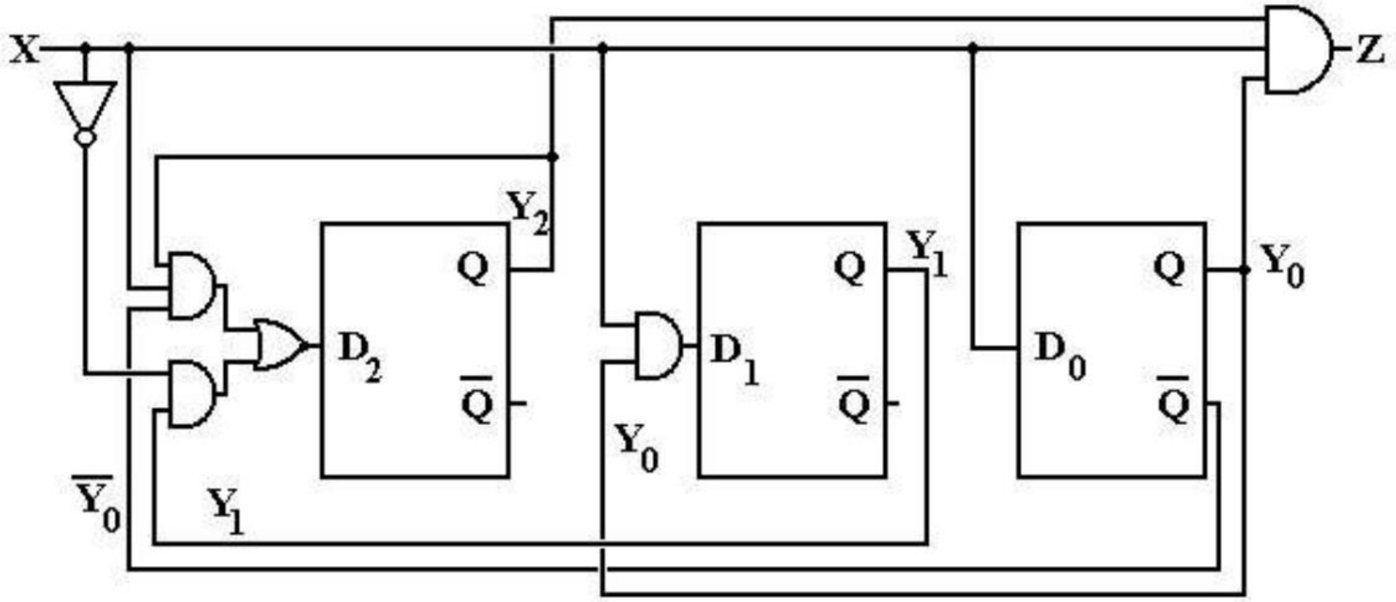
Step 11 – design implemented with D flip-flops




D2 = X’·Y1 + X·Y2·Y0’

D1 = X ·Y0

D0 = X

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1. Design a 11011 sequence detector using JK flip-flops. Allow overlap.

Step 12 – Derive an Input Table for Each JK Flip-Flop using its Excitation Table And Produce the Input Equations for Each Flip-Flop

| $Y_2Y_1Y_0$ | X = 0 | | | X = 1 | | |
|---|---|---|---|---|---|---|
| | $Y_2$ | $J_2$ | $K_2$ | $Y_2$ | $J_2$ | $K_2$ |
| 0 0 0 | 0 | 0 | d | 0 | 0 | d |
| 0 0 1 | 0 | 0 | d | 0 | 0 | d |
| 0 1 1 | 1 | 1 | d | 0 | 0 | d |
| 1 0 0 | 0 | d | 1 | 1 | d | 0 |
| 1 0 1 | 0 | d | 1 | 0 | d | 1 |

X = 0
J2 = Y1
K2 = 1

X = 1
J2 = 0
K2 = Y0

thus, J2 = X’·Y1
thus, K2 = X’ + X·Y0 = X’ + Y0.

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Step 13 – Derive an Input Table for Each JK Flip-Flop using its Excitation Table And Produce the Input Equations for Each Flip-Flop

| $Y_2Y_1Y_0$ | X = 0 | | | X = 1 | | |
|---|---|---|---|---|---|---|
| | $\mathbf{Y_1}$ | $J_1$ | $K_1$ | $\mathbf{Y_1}$ | $J_1$ | $K_1$ |
| 0 **0** 0 | 0 | 0 | d | 0 | 0 | d |
| 0 **0** 1 | 0 | 0 | d | 1 | 1 | d |
| 0 **1** 1 | 0 | d | 1 | 1 | d | 0 |
| 1 **0** 0 | 0 | 0 | d | 0 | 0 | d |
| 1 **0** 1 | 0 | 0 | d | 1 | 1 | d |

X = 0
J1 = 0
K1 = 1

X = 1
J1 = Y0
K1 = 0

thus J1 = X·Y0 and K1 = X’.

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1. Design a 11011 sequence detector using JK flip-flops. Allow overlap.

Step 14 – Derive an Input Table for Each JK Flip-Flop using its Excitation Table And Produce the Input Equations for Each Flip-Flop

| $Y_2Y_1Y_0$ | X = 0 | | | X = 1 | | |
|---|---|---|---|---|---|---|
| | $Y_0$ | $J_0$ | $K_0$ | $Y_0$ | $J_0$ | $K_0$ |
| 0 0 **0** | 0 | 0 | d | 1 | 1 | d |
| 0 0 **1** | 0 | d | 1 | 1 | d | 0 |
| 0 1 **1** | 0 | d | 1 | 1 | d | 0 |
| 1 0 **0** | 0 | 0 | d | 1 | 1 | d |
| 1 0 **1** | 0 | d | 1 | 1 | d | 0 |

X = 0
J0 = 0
K0 = 1

X = 1
J0 = 1
K0 = 0

thus J0 = X and K0 = X', as expected.

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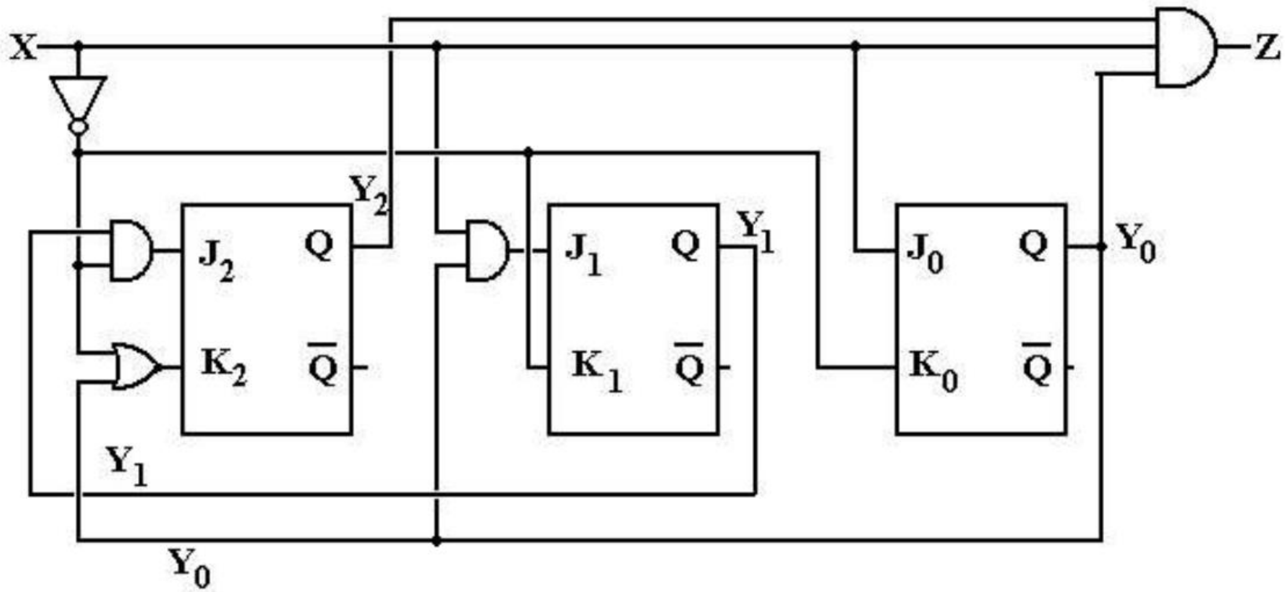
Step 15 – Draw Circuit




The equations implemented in this design are:

$Z = X \cdot Y_2 \cdot Y_0$

$J_2 = X' \cdot Y_1$ $\quad K_2 = X' + Y_0$

$J_1 = X \cdot Y_0$ $\quad K_1 = X'$

$J_0 = X$ $\quad K_0 = X'$