



**BITS Pilani**

Hyderabad Campus

Department of Electrical Engineering



# **Digital Design**

## **First Semester 2020-21**

### **Tutorial : 12**

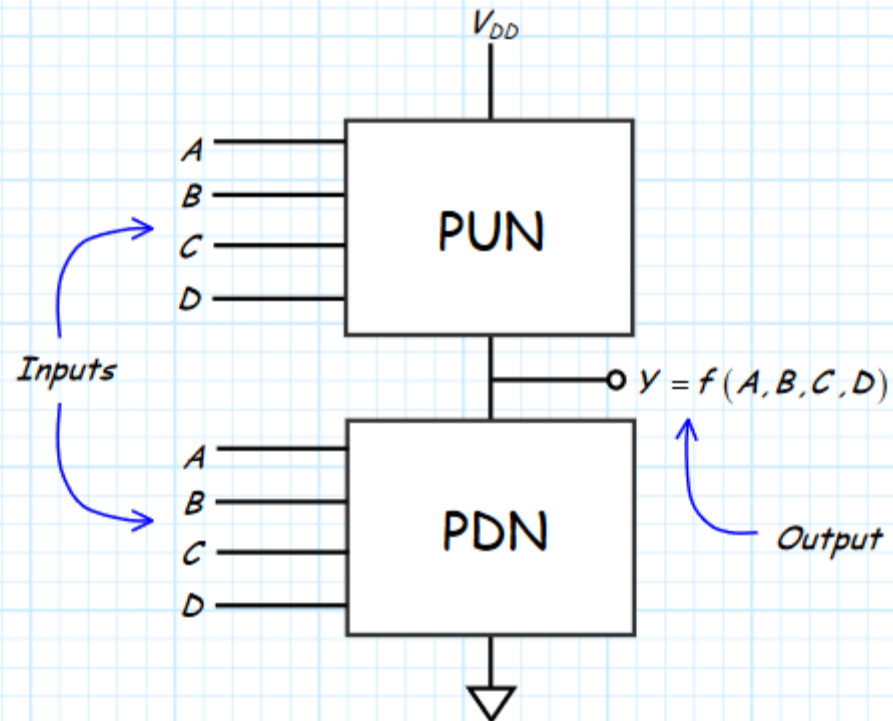
# **CMOS Implementation**

# CMOS Device Structure

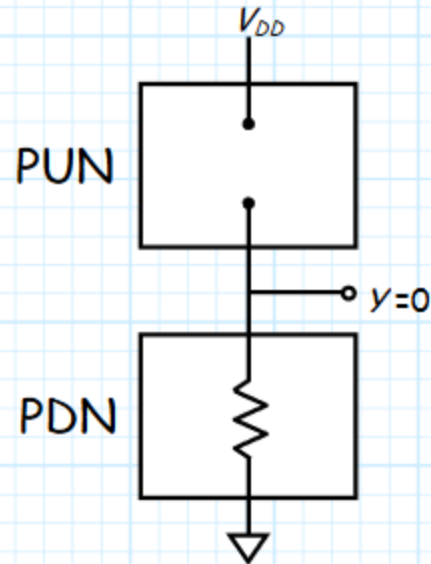
For every CMOS device, there are essentially **two** separate circuits:

- 1) *The Pull-Up Network*
- 2) *The Pull-Down Network*

The basic **CMOS** structure is:

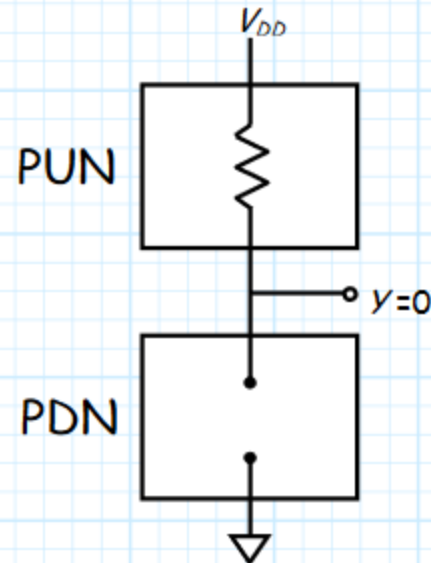


**State 1:** PUN is **open** and PDN is **conducting**.



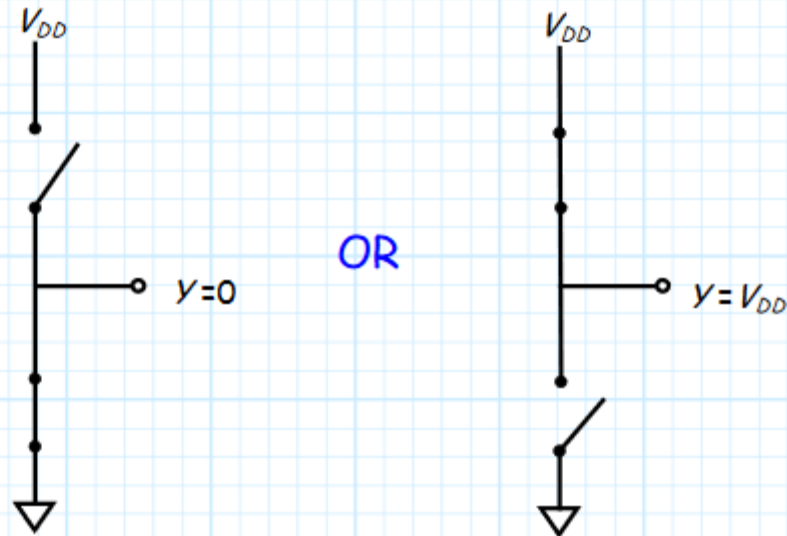
In this state,  
the output is  
**LOW** (i.e.,  $Y=0$ ).

**State 2:** PUN is **conducting** and PDN is **open**.



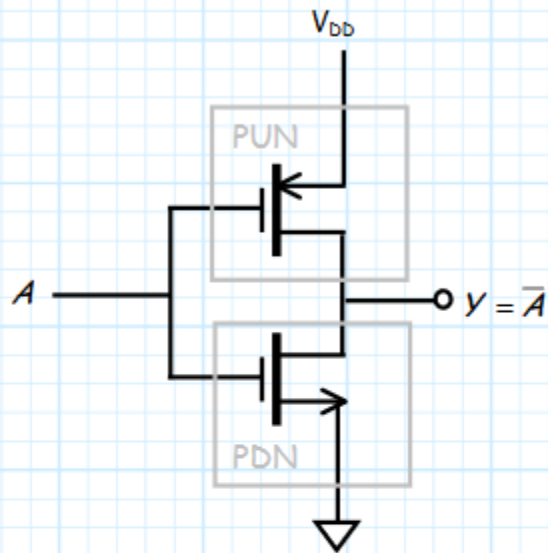
In this state,  
the output is  
**HIGH** (i.e.,  $Y=1$ ).

Thus, the PUN and the PDN essentially act as **switches**, connecting the output to **either**  $V_{DD}$  or to ground:



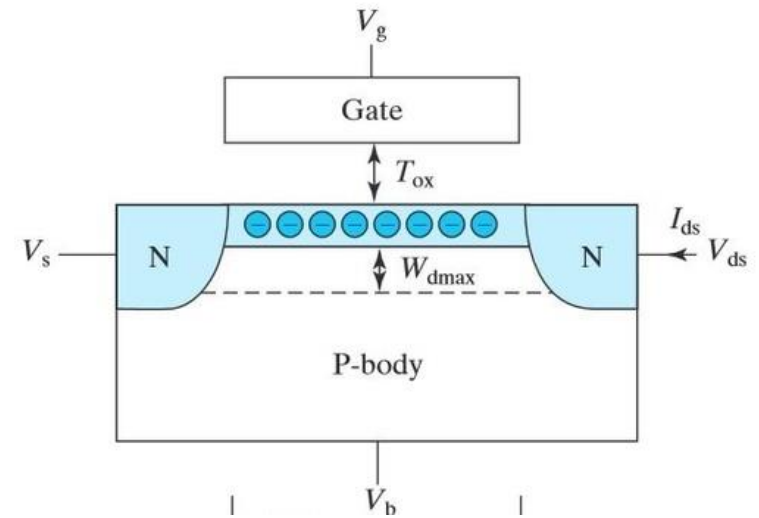
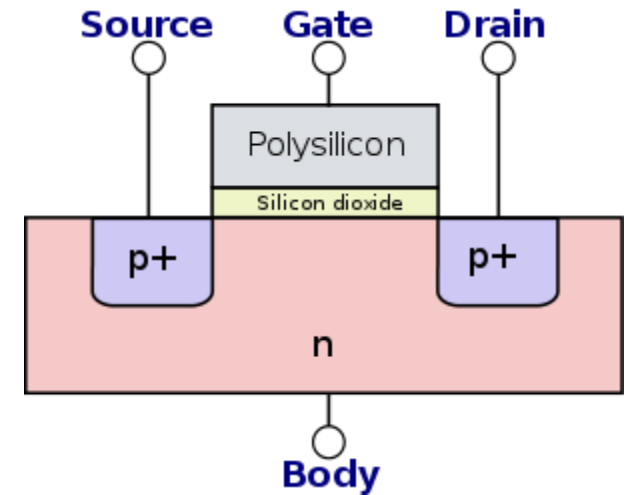
- \* Note that the key to proper operation is that **one** switch must be closed, while the **other** must be open.
- \* **Both** switches closed or **both** switches open would cause an **ambiguous** digital output!
- \* To prevent this from occurring, the PDN and PUN must be **complementary** circuits.

For example, consider the **CMOS inverter**:



For more **complex** digital CMOS gates (e.g., a 4-input OR gate), we find:

- 1) The PUN will consist of **multiple** inputs, therefore requires a circuit with **multiple PMOS** transistors.
- 2) The PDN will consist of **multiple** inputs, therefore requires a circuit with **multiple NMOS** transistors.



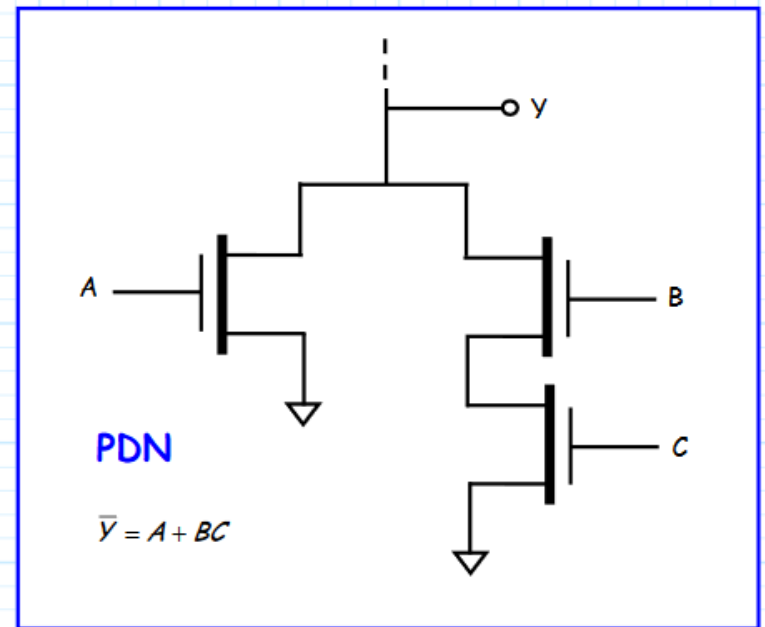
## PDN Design Synthesis

1. If the PDN is **conducting**, then the **output** will be low. Thus, we must find a Boolean expression for the **complemented output**  $\bar{Y}$ .

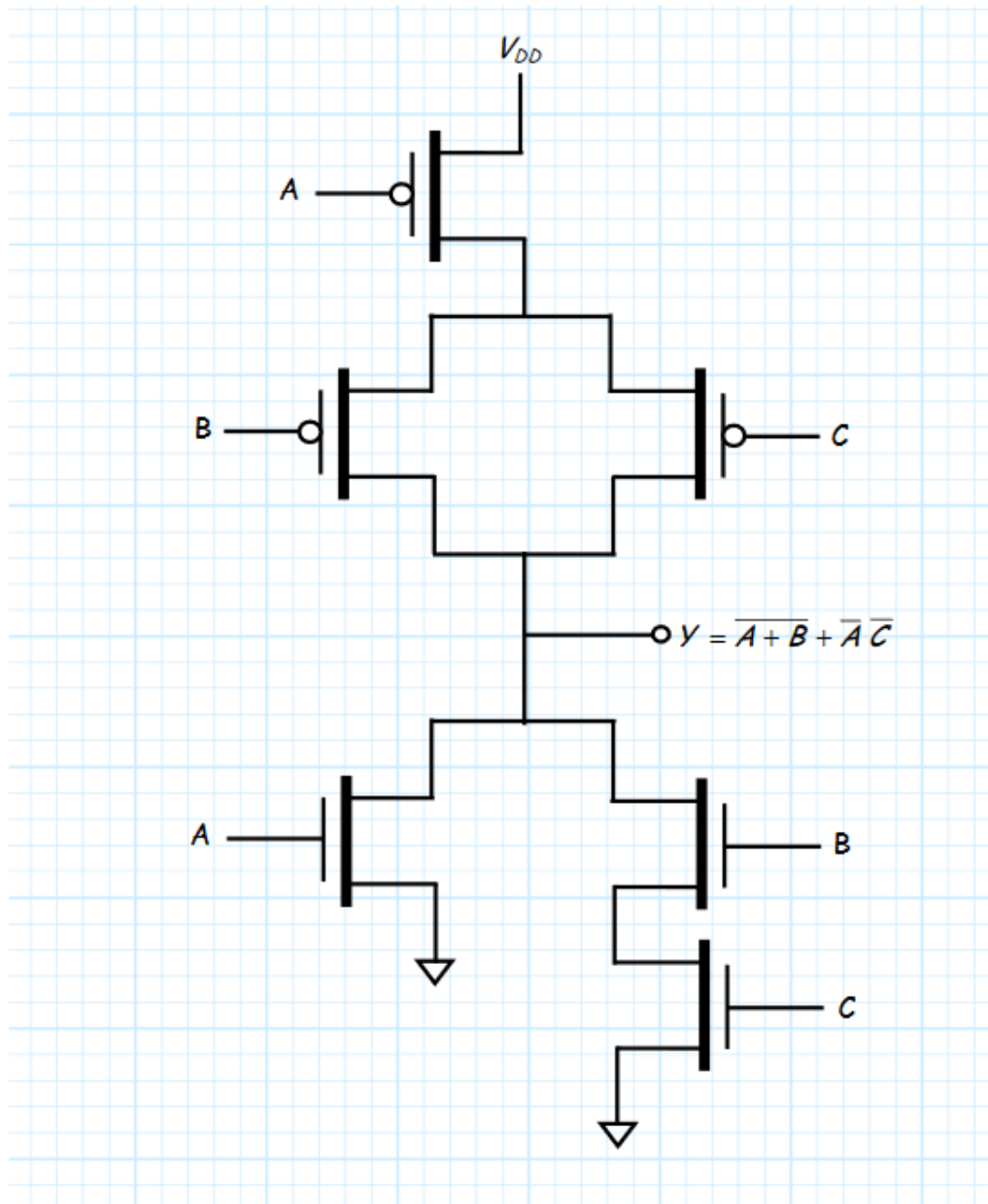
In turn, the PDN can only be conducting if **one or more** of the NMOS devices are **conducting**—and NMOS devices will be conducting (i.e., **triode mode**) when the **inputs are high** ( $V_{GSN} = V_{DD}$ ).

Thus, we **must** express  $\bar{Y}$  in terms of **un-complemented inputs**  $A, B, C$ , etc (i.e.,  $\bar{Y} = f(A, B, C)$ ).

$$\text{e.g., } \rightarrow \bar{Y} = A + BC$$









# Problem 1

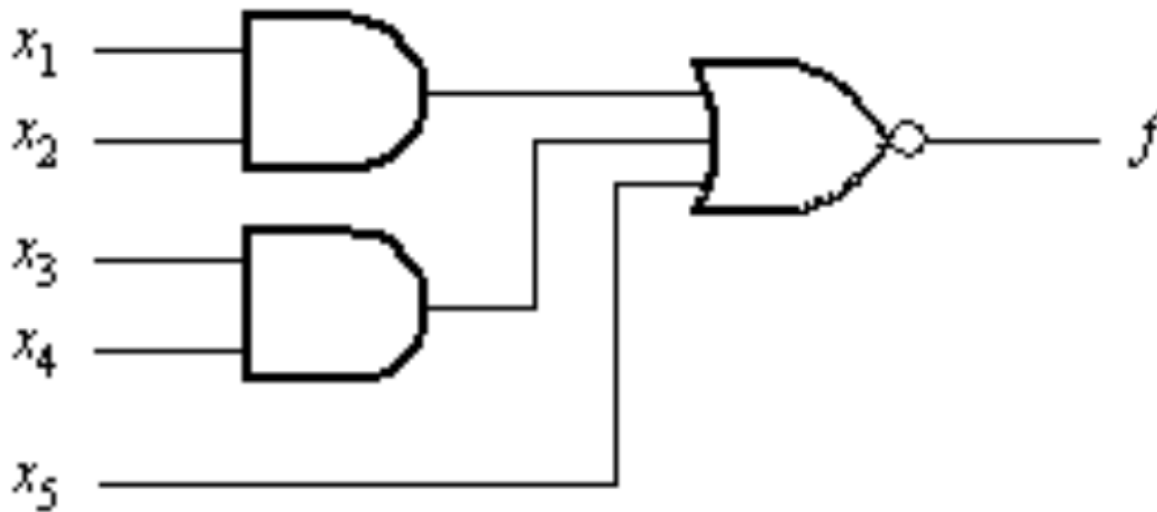
1. Realize the following logic function with AOI gates and CMOS Transistors

$$f = \overline{x_1x_2 + x_3x_4 + x_5}.$$

# Problem 1

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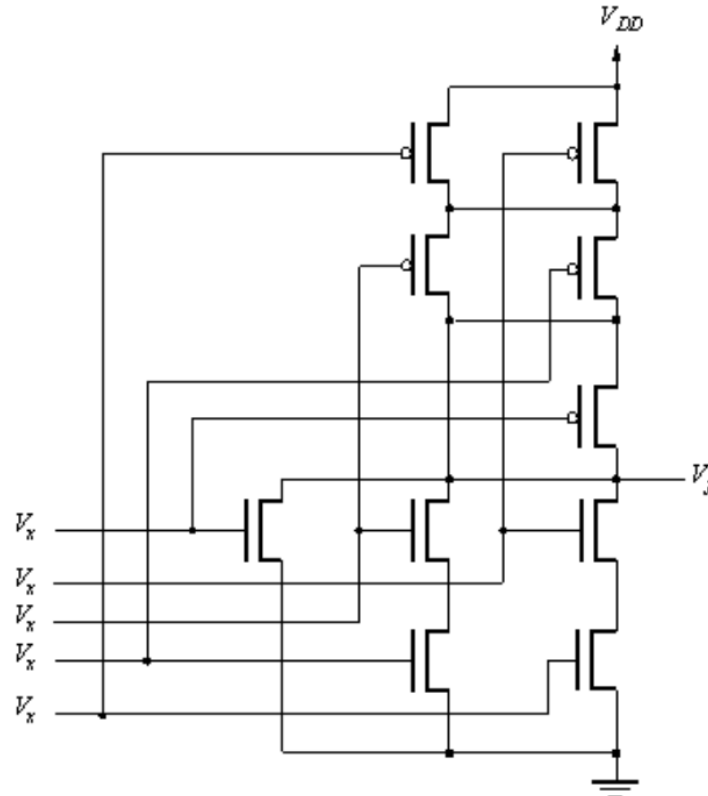
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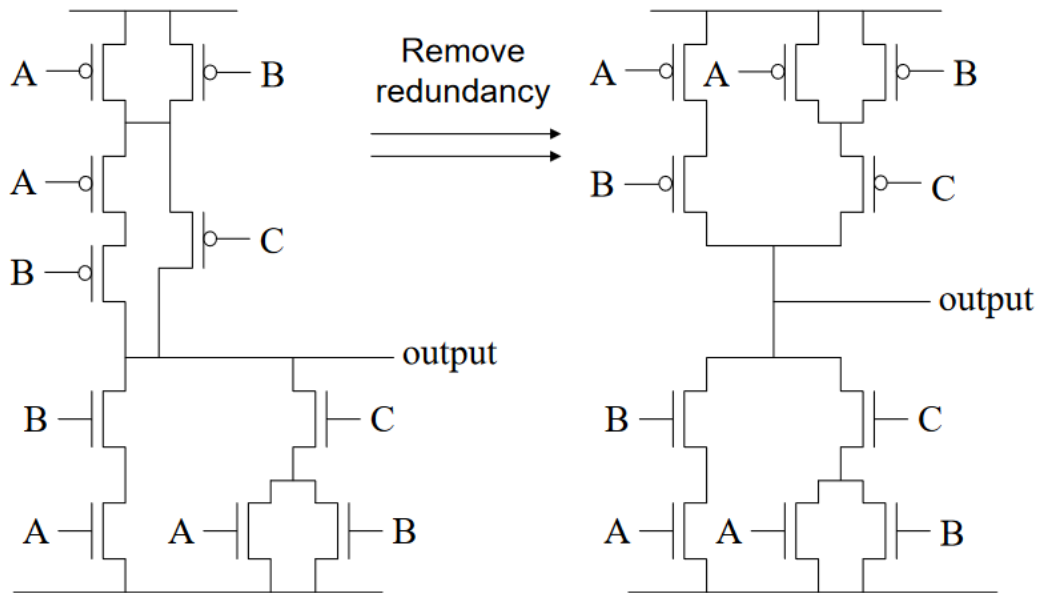
$$f = \overline{x_1x_2 + x_3x_4 + x_5}$$



# Problem 2

## 2. Realize Full Adder with CMOS Transistors

$$F = \overline{((A.B) + C.(A+B))} = \text{carry}$$

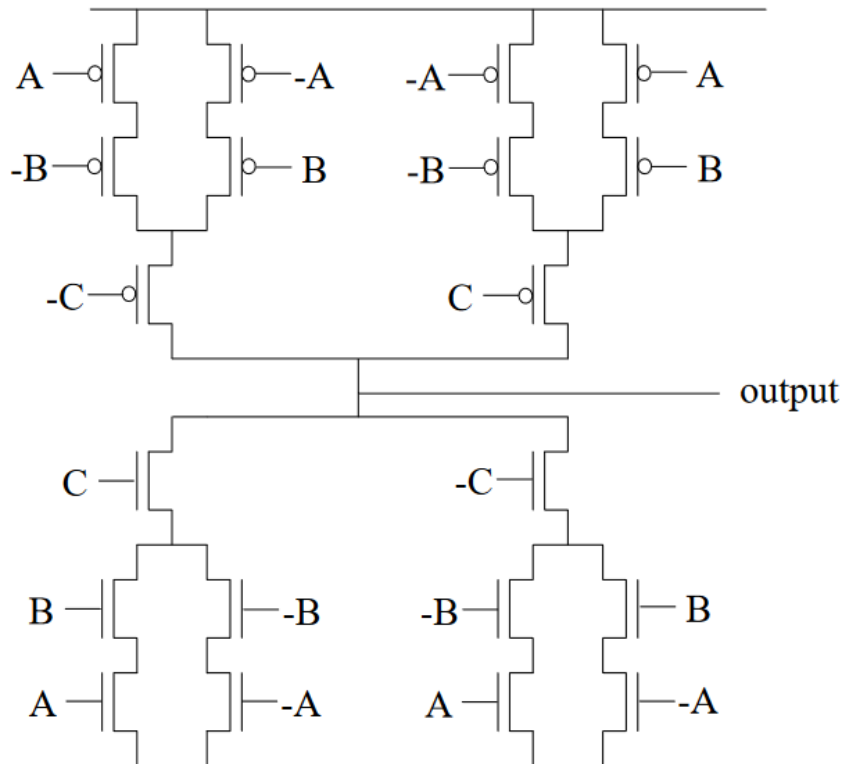


Symmetrical !

# Problem 2

## 2. Realize Full Adder with CMOS Transistors

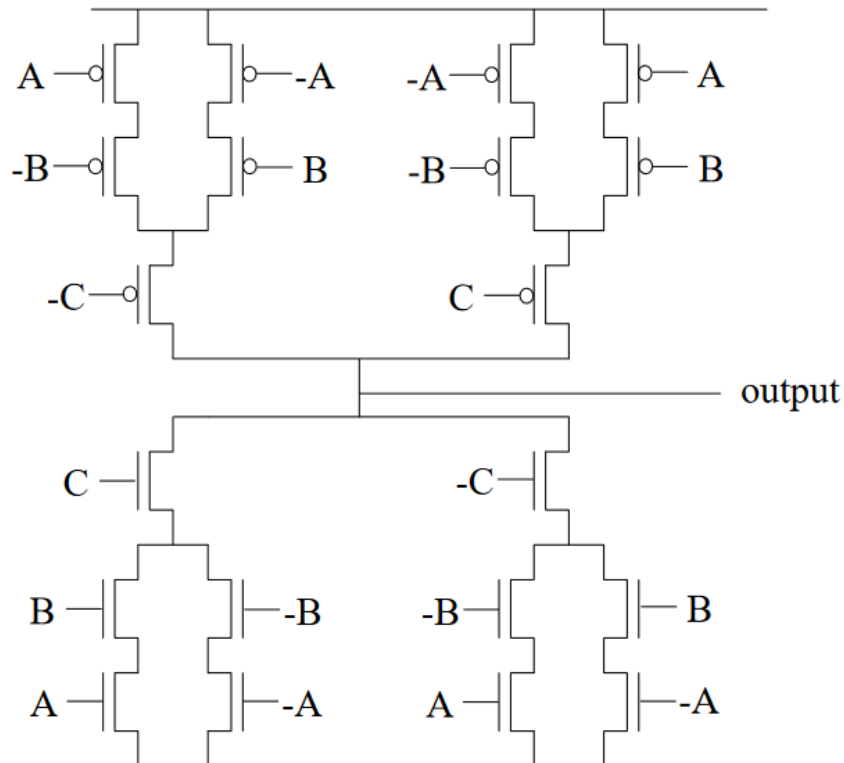
$$F = \overline{(ABC + \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + A\overline{B}\overline{C})} = \overline{\text{sum}}$$



# Problem 2

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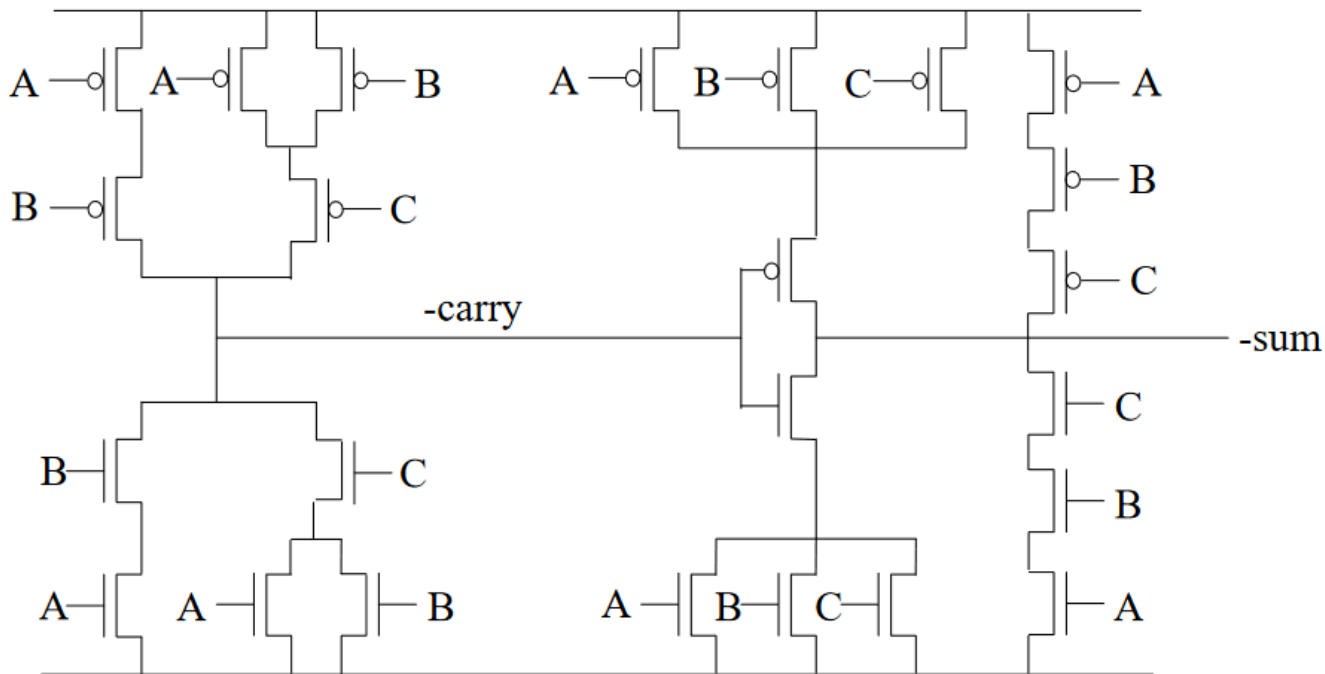
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Full Adder Circuit



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