BITS Pilani
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Department of Electrical Engineering

Digital Design
First Semester 2020-21
Tutorial : 10

State Table Reduction

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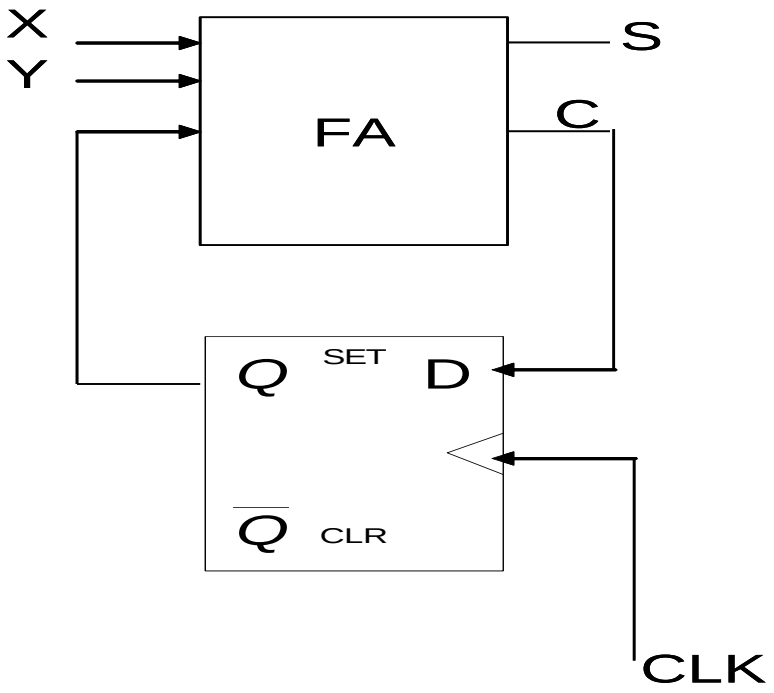
1. A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown. Derive the state table and state diagram of the sequential circuit.



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2. Reduce the number of states in the following table and tabulate the reduced state table.

PRESENT STATE	NEXT STATE		OUTPUT	
	X=0	X=1	X=0	X=1
a	f	b	0	0
b	d	c	0	0
c	f	b	0	0
d	g	a	1	0
f	f	b	1	1
g	g	d	0	1

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3. Optimize using Implication Table .

State Table to be Reduced.

Present State	Next State		Output	
	x=0	x=1	x=0	x=1
a	d	a	0	0
b	e	a	0	0
c	g	f	0	1
d	a	d	1	0
e	a	d	1	0
f	c	b	0	0
g	a	e	1	0