Digital Electronics and Computer Organization

Digital Design

Lecture 26: Programable Logic Devices

Birla Institute of Technology & Science, Pilani
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Types of PLD

Programable Logic Array (PLA)

Programable Array Logic Array (PAL)

Simple Programmable Logic Device (SPLD)

Complex Programmable Logic Device (CPLD)

Field Programmable Gate Arrays (**FPGAs**)

PLA

Programmable device capable of implementing functions expressed in SOP.

- Consists of input buffers and inverters followed by:
- Programmable AND plane, followed by
- Programmable OR plane.
- Can implement m logic functions of n variables. Limit is the number of product terms that can be generated inside of the device.

PLA

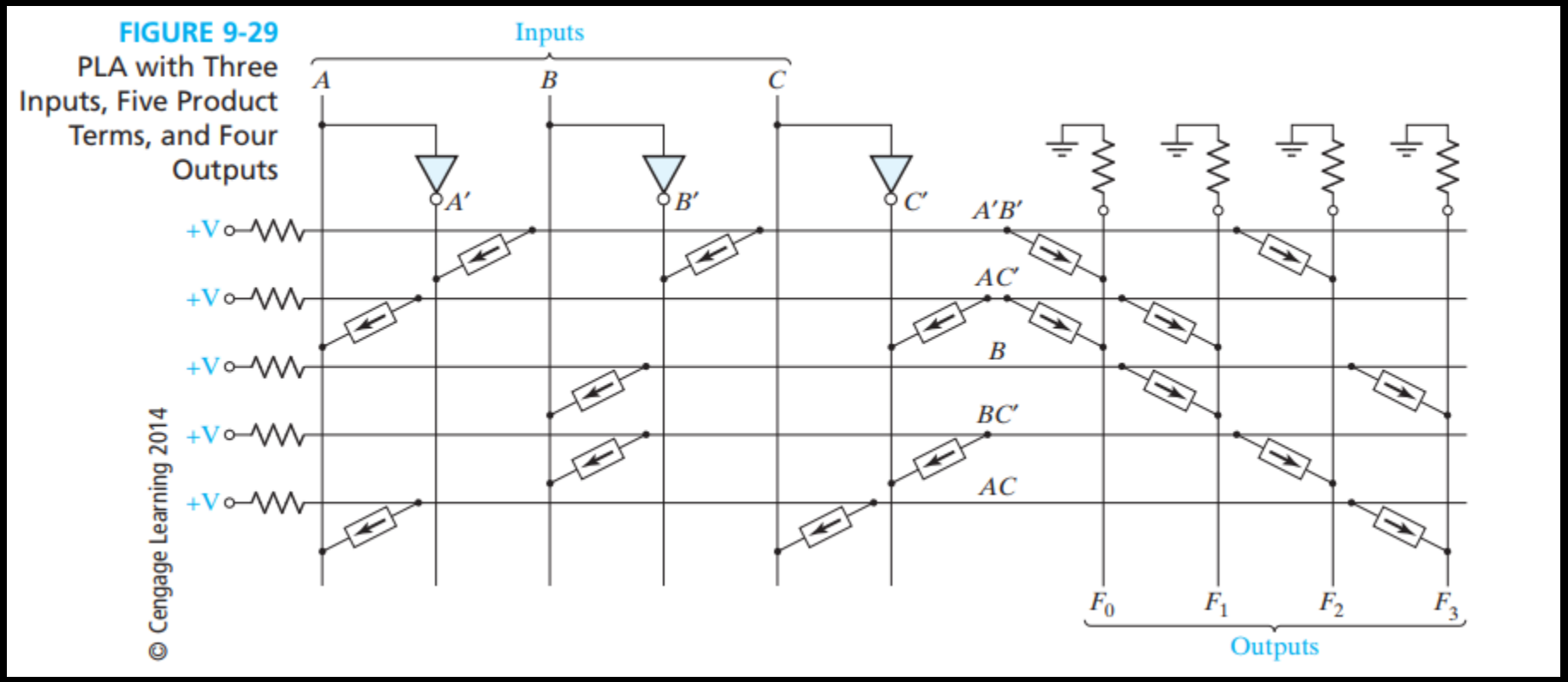
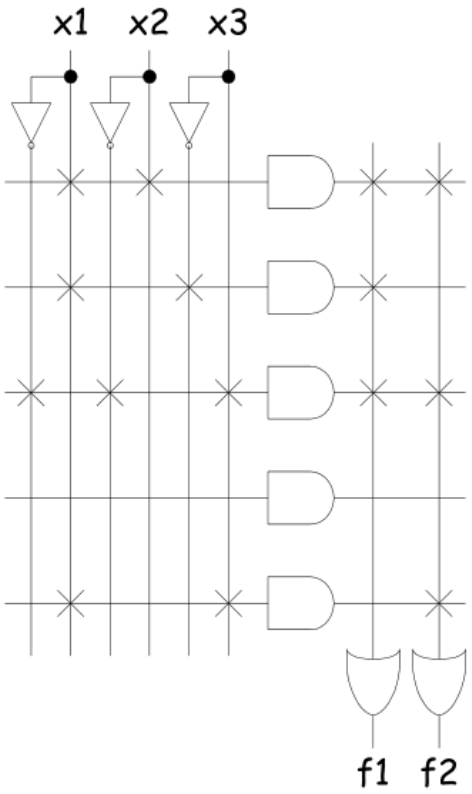


FIGURE 9-29
PLA with Three Inputs, Five Product Terms, and Four Outputs

PLA

- Example implementing 2 logic functions of 3 inputs using a **3-5-2 PLA**.



$$f_1 = x_1x_2 + x_1\overline{x}_3 + \overline{x}_1\overline{x}_2x_3$$

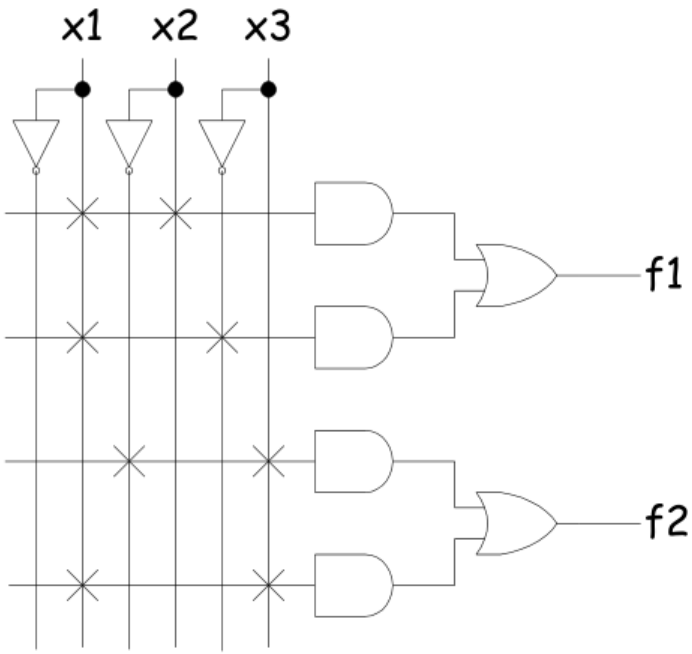
$$f_2 = x_1x_2 + \overline{x}_1\overline{x}_2x_3 + x_1x_3$$

PAL

- Similar to a PLA, but only has a programmable AND plane.
  - The OR plane is fixed.
- Not as flexible as a PLA since only certain AND gates feed each OR gate, but has fewer things that need programming.

PAL

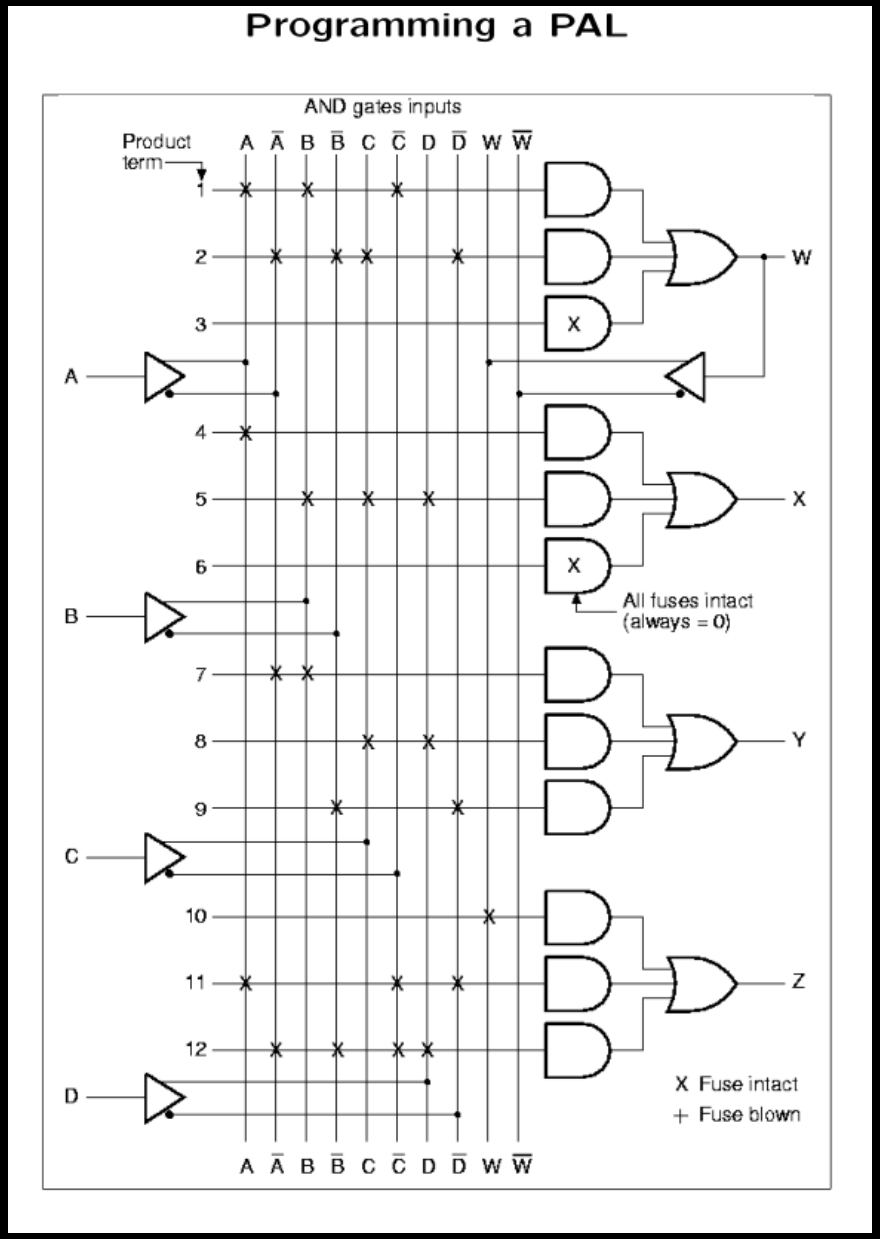
- Example of a PAL:



$$f_1 = x_1x_2 + x_1\overline{x}_3$$

$$f_2 = \overline{x}_2x_3 + x_1x_3$$

PAL


Programming a PAL
AND gates inputs
Product term
A Ā B B̄ C C̄ D D̄ W W̄
1
2
3
4
5
6
7
8
9
10
11
12
W
X
Y
Z
All fuses intact (always = 0)
X Fuse intact
+ Fuse blown

Programmable Array Logic

Example

$W(A, B, C, D) = \sum (2, 12, 13)$

$X(A, B, C, D) = \sum (7,8,9,10,11,12,13,14,15)$

$Y(A, B, C, D) = \sum (1,2,8,12,13)$

$W(A, B, C, D) = ABC' + A'B'CD'$

$X(A, B, C, D) = A + BCD$

$Y(A, B, C, D) = ABC' + A'B'CD' + AC'D' + A'B'C'D$

$= W + AC'D' + A'B'C'D$

Programmable Array Logic

Example

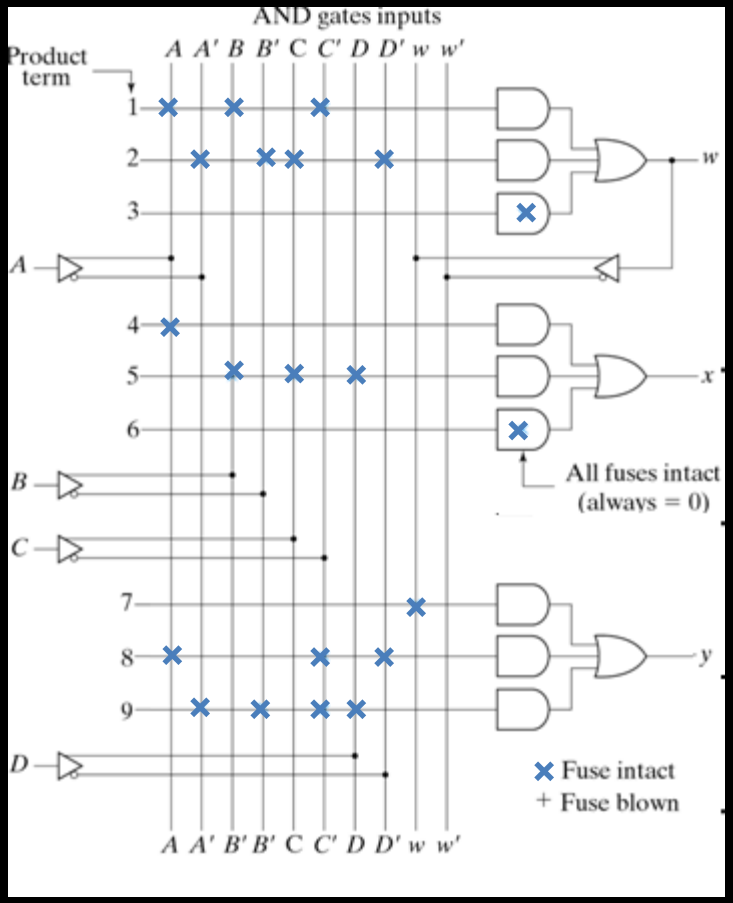
W(A, B, C, D) = ABC' + A'B'CD'

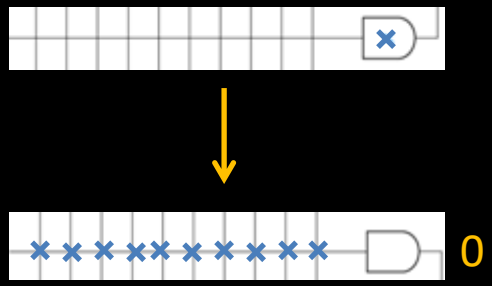
X(A, B, C, D) = A + BCD

Y(A, B, C, D) = W + AC'D' + A'B'C'D

Product	AND Inputs					Outputs	
	A	B	C	D	w		
1	1	1	0	--	--	W = ABC' + A'B'CD'	Section 1
2	0	0	1	0	--		
3	--	--	--	--	--		
4	1	--	--	--	--	X = A + BCD	Section 2
5	--	1	1	1	--		
6	--	--	--	--	--		
7	--	--	--	--	1	Y = W + AC'D' + A'B'C'D	Section 3
8	1	--	0	0	--		
9	0	0	0	1	--		

Programmable Array Logic





Example

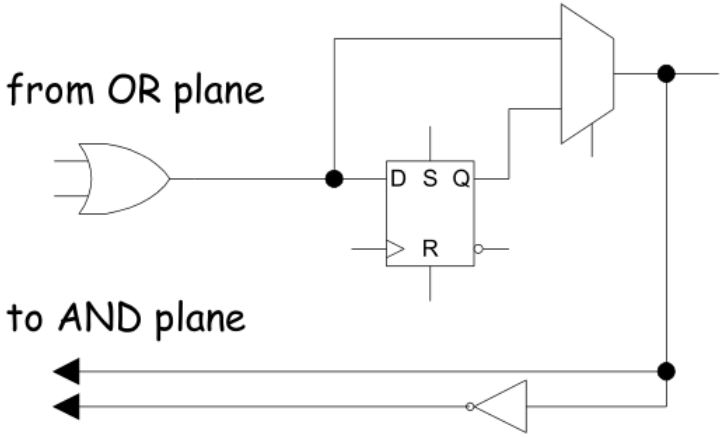
W(A, B, C, D) = ABC’ + A’B’CD’

X(A, B, C, D) = A + BCD

Y(A, B, C, D) = W + AC’D’ + A’B’C’D

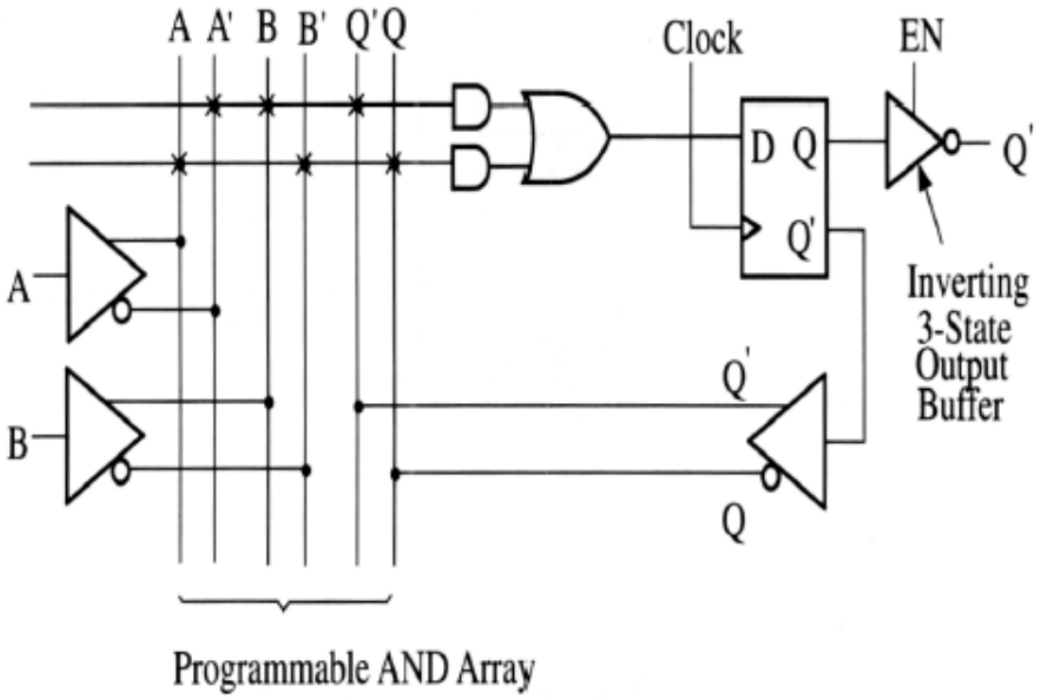
Simple Programmable Logic Device (SPLD)

- To implement sequential circuits, take a PAL and add some flip-flops at the output of the OR plane.
- For example…



- Above circuit (plus SOP from the AND plane and OR gate) form a **MacroCell**.
- Several **MacroCells** together in the same IC is called an SPLD.

Registered (Sequential) PAL:



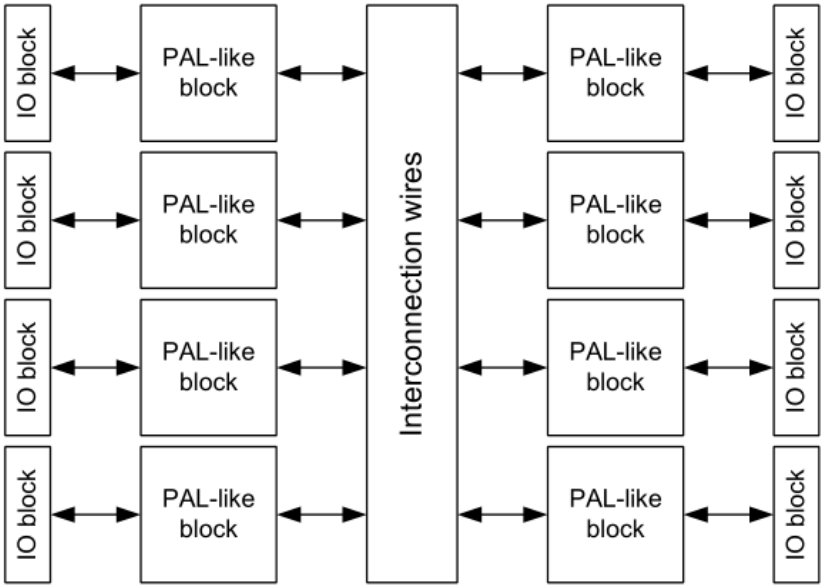
$$Q^{+}=D=A'BQ'+AB'Q$$

Complex Programmable Logic Device (CPLD)

- PLA, PAL and SPLD typically contain small number of outputs (e.g., 16 outputs) with many inputs (e.g., 36 inputs) and a fair number of product terms.
  - Therefore only good for simple circuits where each equation has a wide fanin.
- Using a **Complex Programmable Logic Device (CPLD)** is the "next step" if we have a large complicated circuit…
- CLPD consists of many SPLD connected together by a **Programmable Routing Fabric** all in the **same** IC.

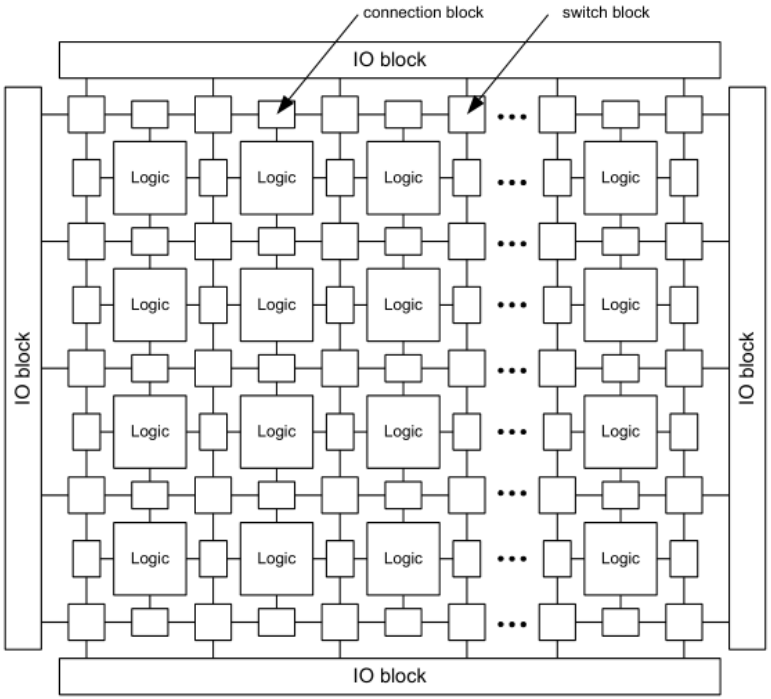
Complex Programmable Logic Device (CPLD)

- Typical architecture (each PAL-like block has many inputs – e.g., 36 - , many product terms – e.g., 80 – and several outputs – e.g., 16).

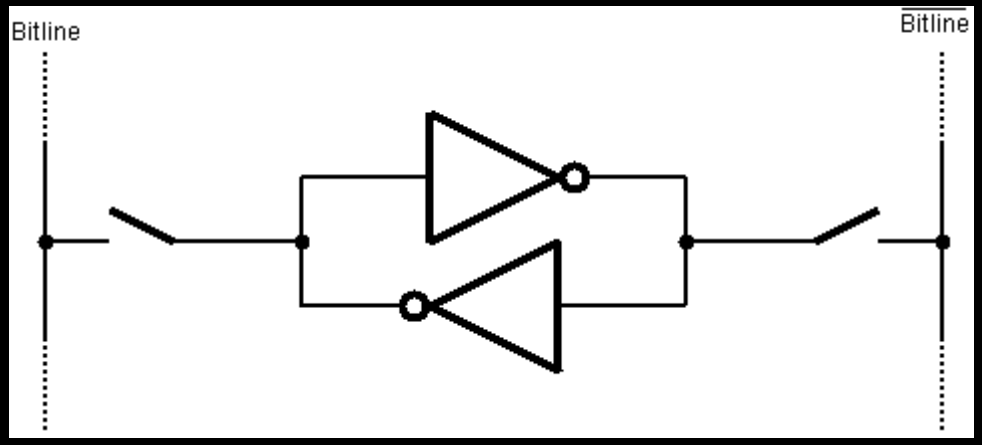


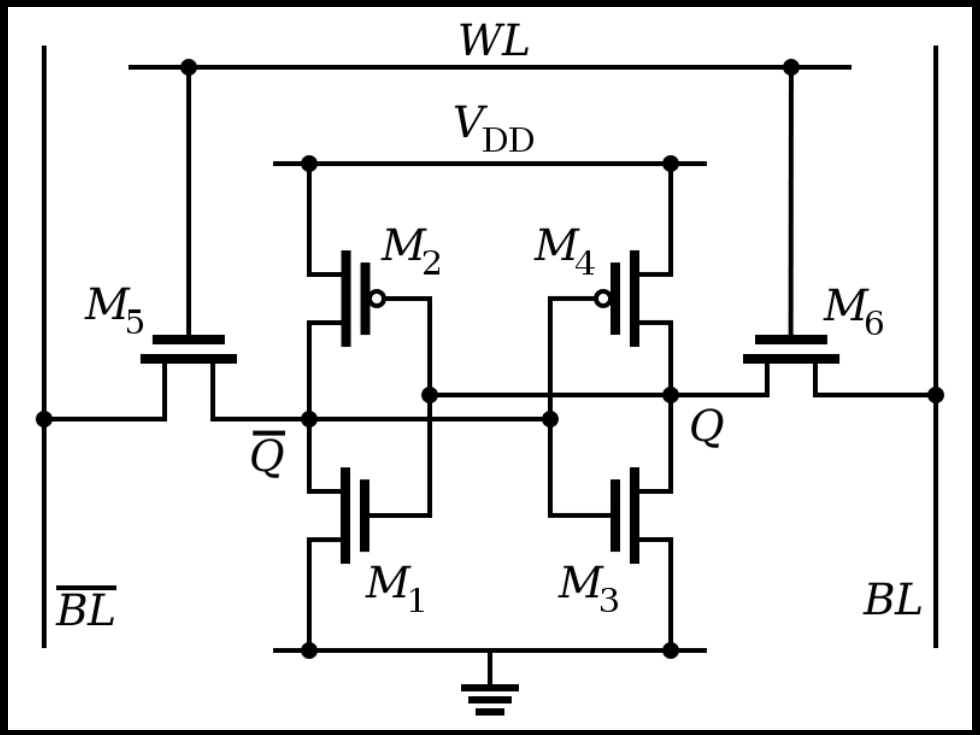
Field Programmable Gate Array (FPGA)

- Typical FPGA consists of many small logic blocks interconnected by programmable routing resources.



SRAM


Bitline
Bitline


WL
V_{DD}
M_2
M_4
M_5
M_6
Q
$\overline{Q}$
M_1
M_3
$\overline{BL}$
BL

Thank You