

Digital Electronics and Computer Organization

Digital Design

Lecture 19: Sequence Detector



Birla Institute of Technology & Science, Pilani
Hyderabad Campus

11/6/2020

Innovate

achieve

1

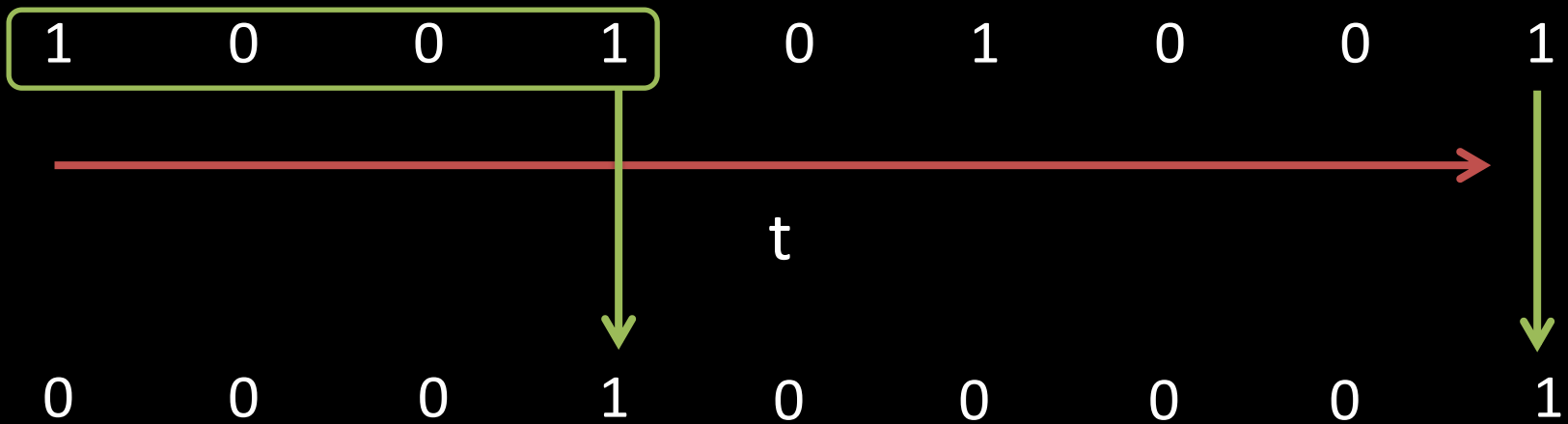
lead



Design of Clocked sequential Circuits

Design of sequence detector (1001)

Bit stream as input

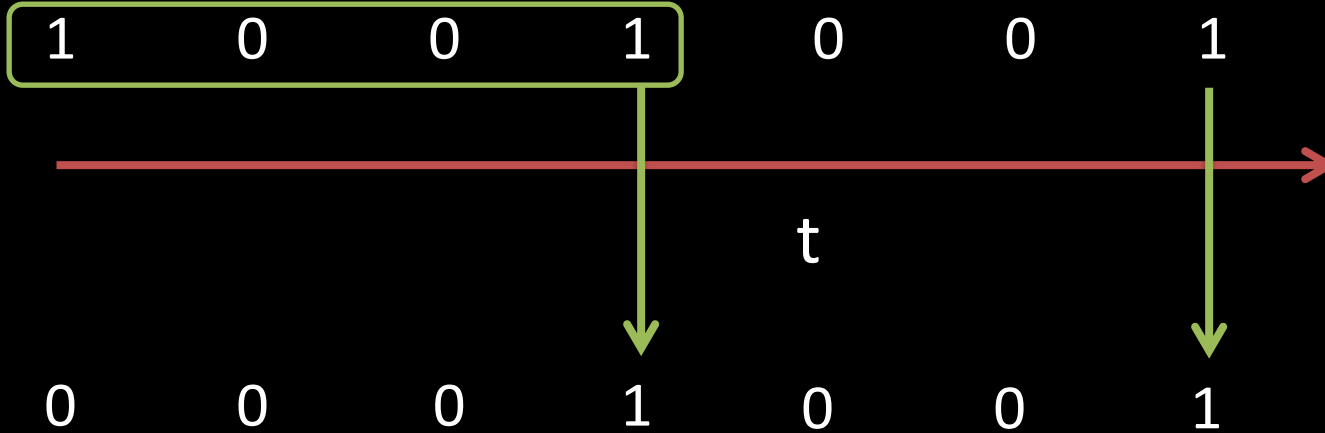




Design of Clocked sequential Circuits

Design of sequence detector (1001)

Overlapping

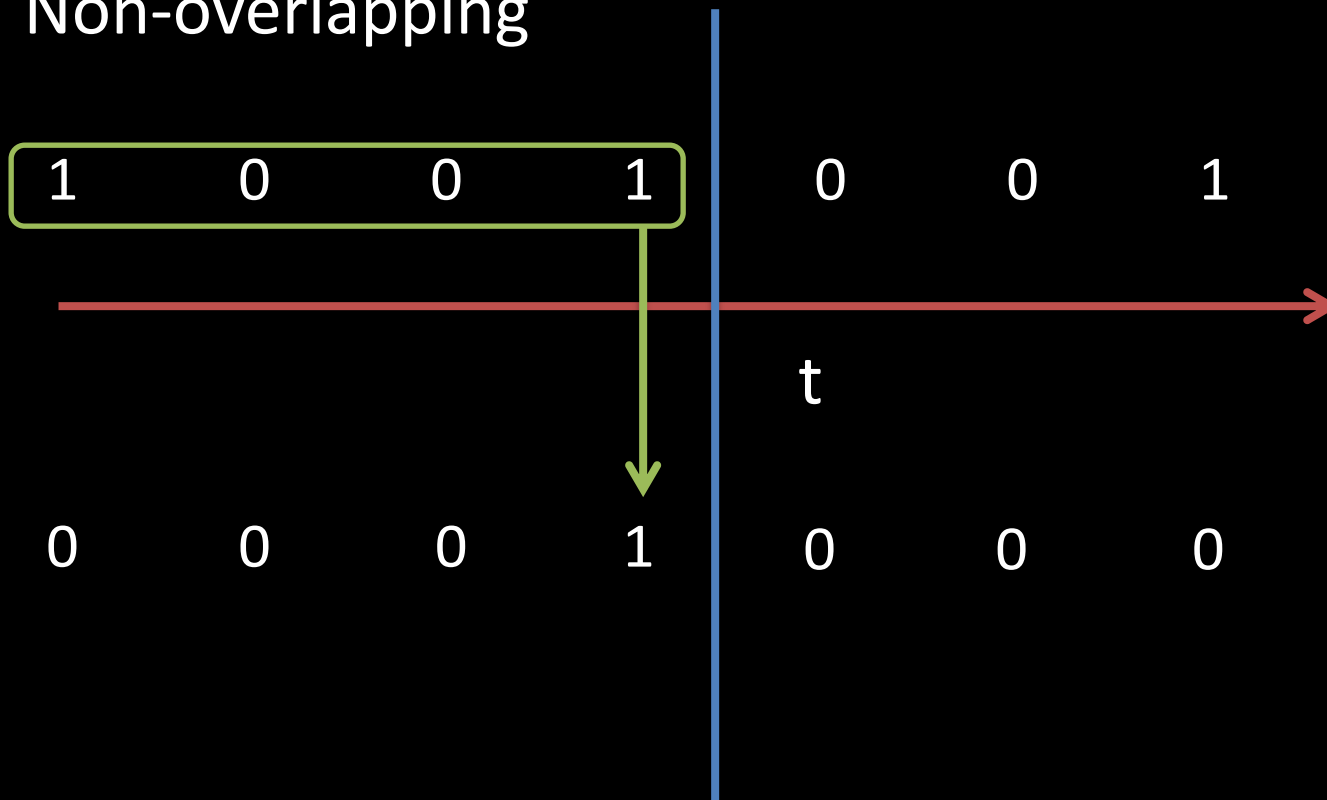




Design of Clocked sequential Circuits

Design of sequence detector (1001)

Non-overlapping





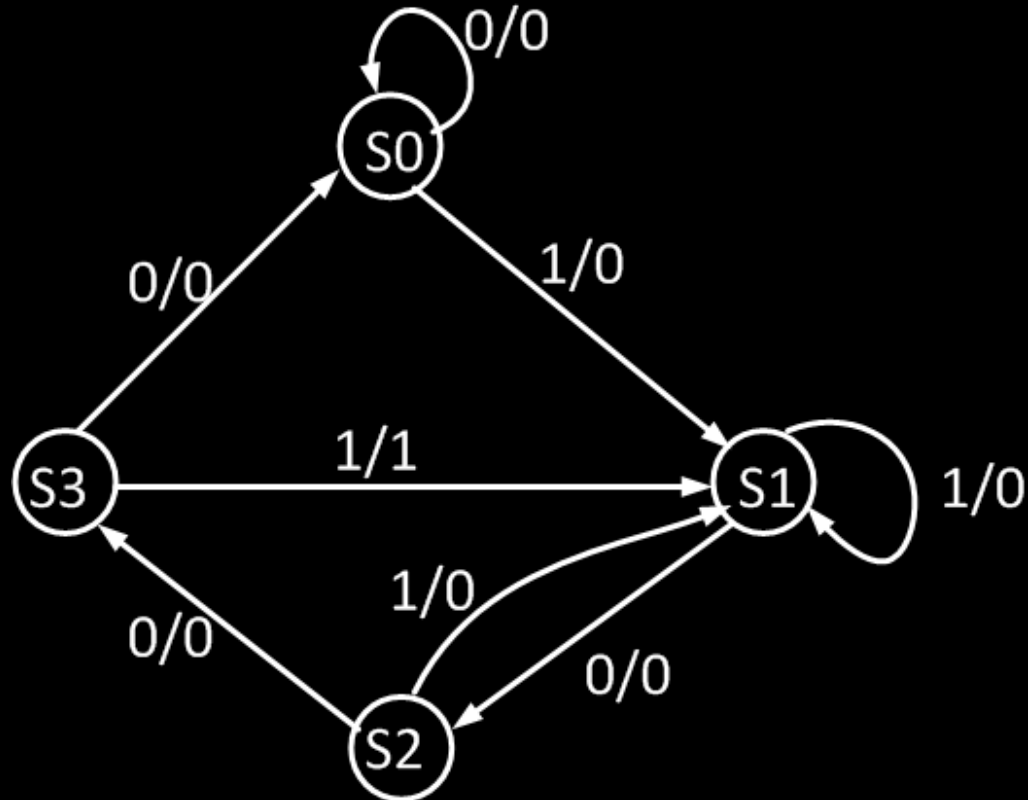
Design of Clocked sequential Circuits

Design of sequence detector overlapping (1001)



Design of Clocked sequential Circuits

Design of sequence detector overlapping (1001)



S0 – 00

S1 – 01

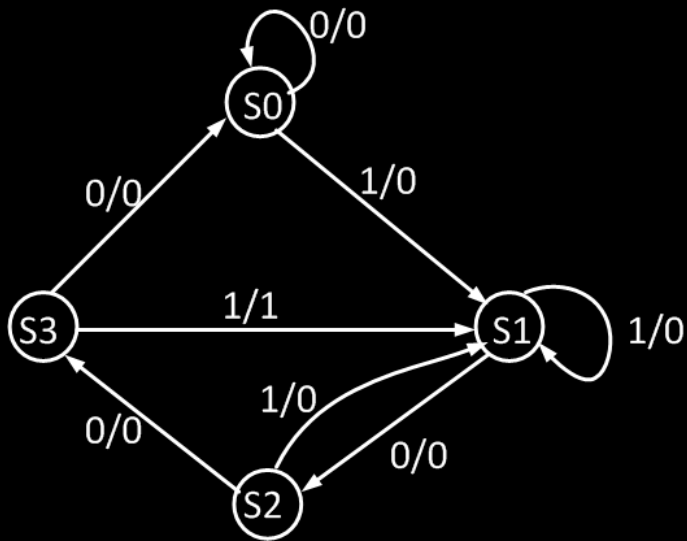
S2 – 10

S3 – 11



Design of Clocked sequential Circuits

Design of sequence detector overlapping (1001)



S0 – 00
 S1 – 01
 S2 – 10
 S3 – 11

Present State		in		Next State			Out
	Q_A	Q_B	X		$Q_{A(t+1)}$	$Q_{B(t+1)}$	Y
S0	0	0	0	S0	0	0	0
S0	0	0	1	S1	0	1	0
S1	0	1	0	S2	1	0	0
S1	0	1	1	S1	0	1	0
S2	1	0	0	S3	1	1	0
S2	1	0	1	S1	0	1	0
S3	1	1	0	S0	0	0	0
S3	1	1	1	S1	0	1	1



Design of Clocked sequential Circuits



Present State		in	Next State		Out		
	Q_A	Q_B	X		$Q_{A(t+1)}$	$Q_{B(t+1)}$	Y
S0	0	0	0	S0	0	0	0
S0	0	0	1	S1	0	1	0
S1	0	1	0	S2	1	0	0
S1	0	1	1	S1	0	1	0
S2	1	0	0	S3	1	1	0
S2	1	0	1	S1	0	1	0
S3	1	1	0	S0	0	0	0
S3	1	1	1	S1	0	1	1

D_A	D_B
0	0
0	1
1	0
0	1
1	1
0	1
0	0
0	1

$$D_A = Q_A'Q_B'X' + Q_AQ_B'X'$$

$$D_B = X + Q_AQ_B'$$

$$Y = Q_AQ_BX$$



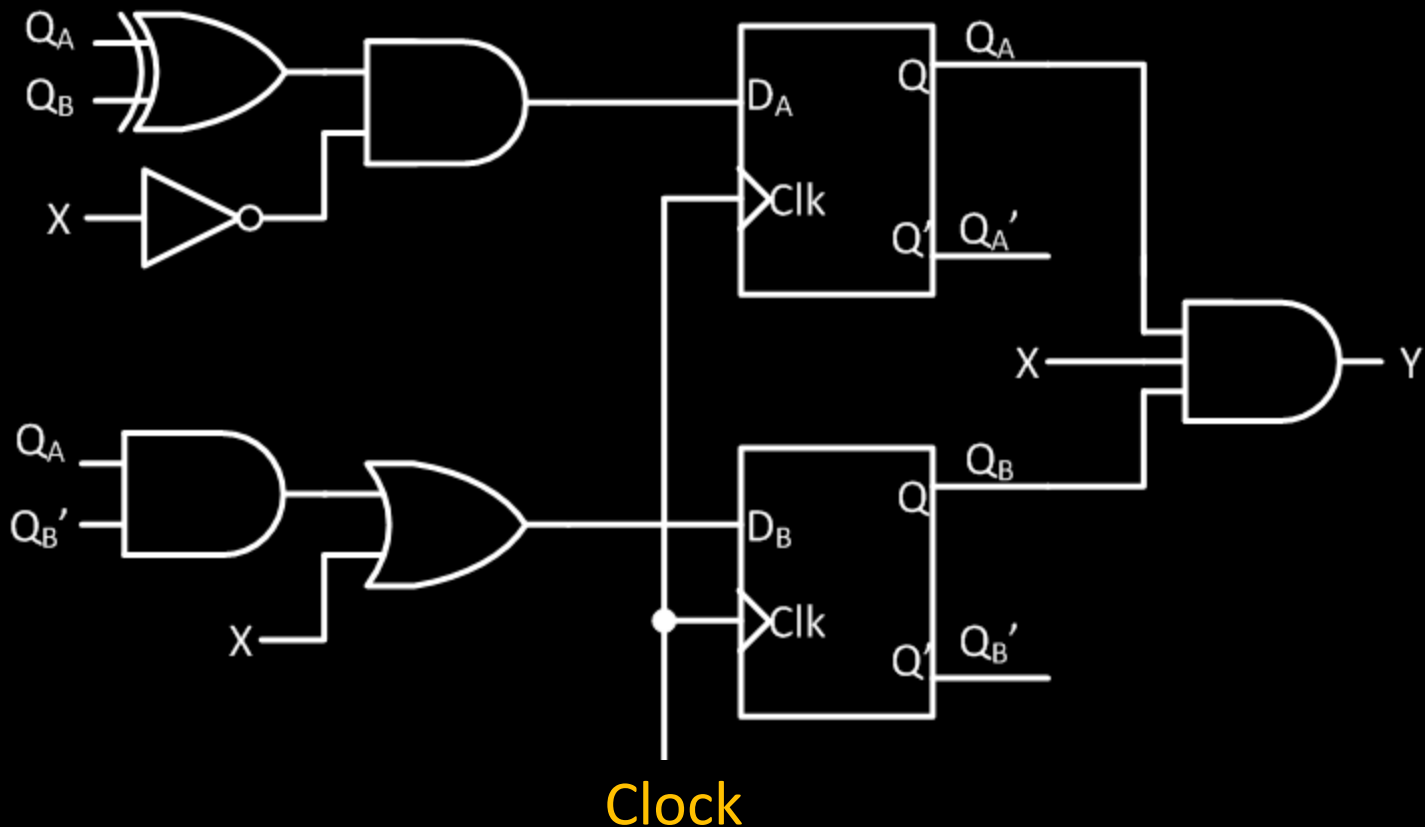
Design of Clocked sequential Circuits



$$D_A = Q_A'Q_BX' + Q_AQ_B'X' = (Q_A \oplus Q_B) X'$$

$$Y = Q_AQ_BX$$

$$D_B = X + Q_AQ_B'$$





Design of Clocked sequential Circuits



Present State			in	Next State			Out
	Q_A	Q_B	X		$Q_{A(t+1)}$	$Q_{B(t+1)}$	Y
S0	0	0	0	S0	0	0	0
S0	0	0	1	S1	0	1	0
S1	0	1	0	S2	1	0	0
S1	0	1	1	S1	0	1	0
S2	1	0	0	S3	1	1	0
S2	1	0	1	S1	0	1	0
S3	1	1	0	S0	0	0	0
S3	1	1	1	S1	0	1	1

J_A	K_A
0	X
0	X
1	X
0	X
X	0
X	1
X	1
X	1

J_B	K_B
0	X
1	X
X	1
X	0
1	X
1	X
X	1
X	0

$$J_A = Q_B X' \quad K_A = Q_B + X$$

$$Y = Q_A Q_B X$$

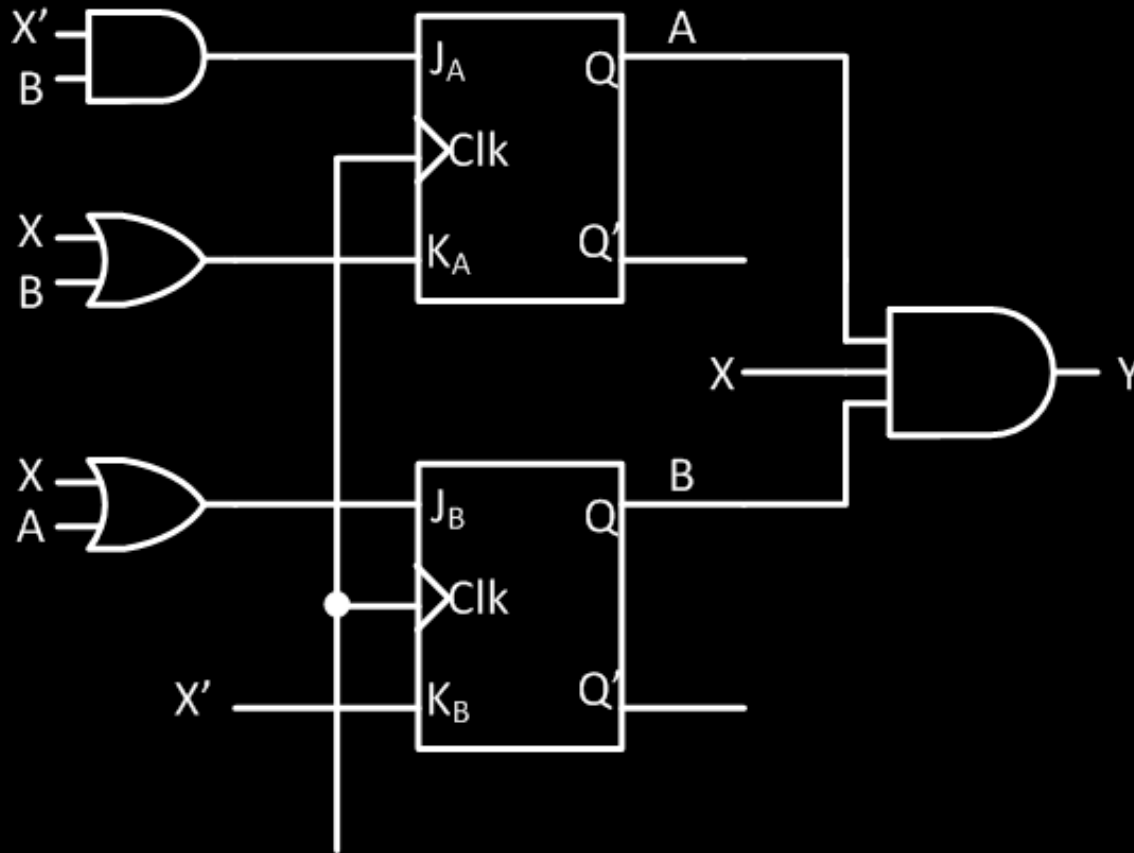
$$J_B = Q_A + X \quad K_B = X'$$



Design of Clocked sequential Circuits



Design of sequence detector overlapping (1001)- JK Flip-flop





Next class

State Reduction



Thank You