Digital Electronics and Computer Organization

Digital Design

Lecture 15: Sequential Logic & SR Latch

Sequential Circuits

Combinational circuits – The outputs are entirely dependent on current inputs

Sequential circuits

– The outputs are dependent on current inputs as well as present state of storage elements

Next state = external inputs + present state

Sequential Circuits

Classification

Synchronous Sequential circuits

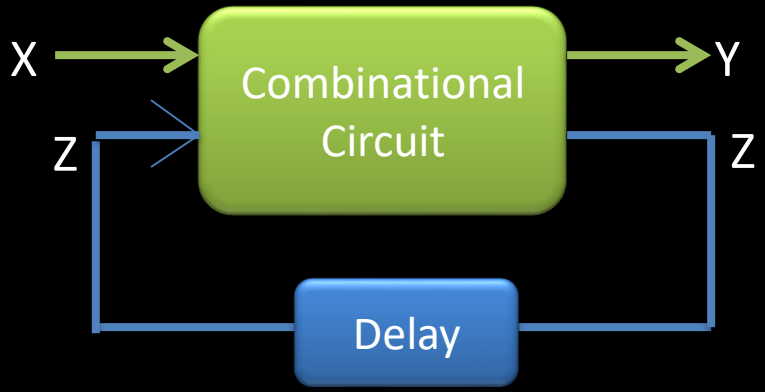
Asynchronous Sequential circuits

Sequential Circuits

Asynchronous sequential circuits

The transition from one state to another is initiated by the change in the primary inputs there is no external synchronization

The memory commonly used are time-delayed devices



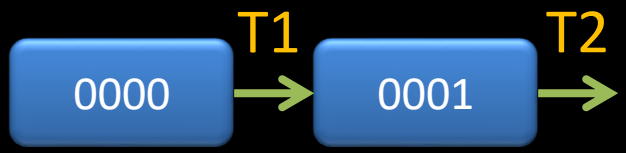
May be regarded as combinational circuits with feedback.

May become unstable

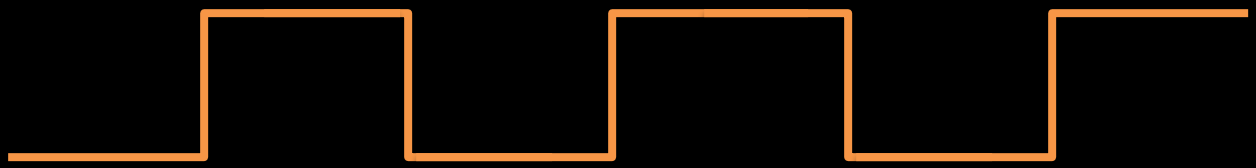
Sequential Circuits

Synchronous sequential circuit

Synchronous sequential circuits change their states and output values at discrete instants of time

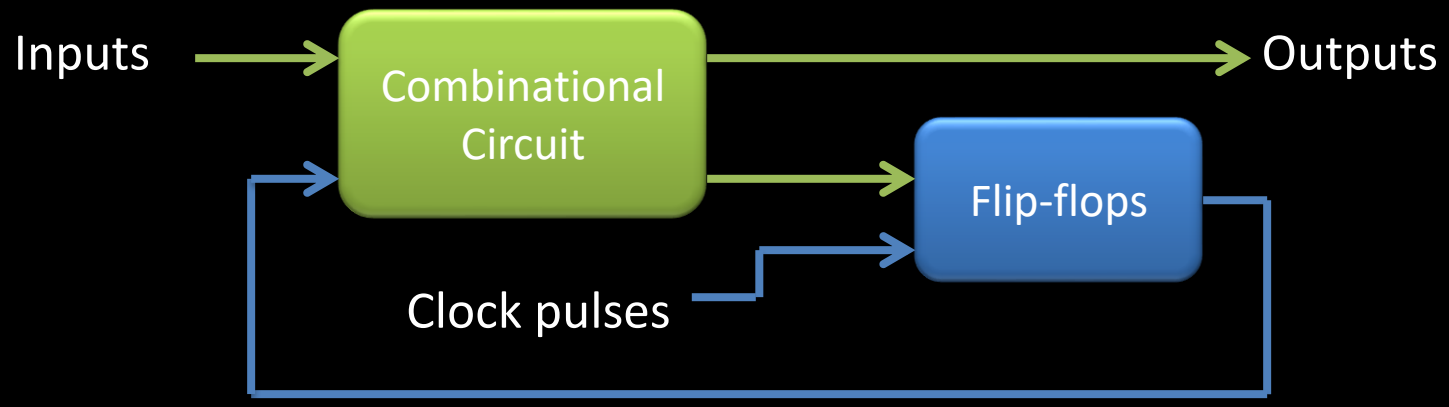


Synchronization is achieved by a timing device called clock generator



Clock generator generates a clock signal having the form of a periodic train of pulses

Sequential Circuits



Clocked synchronous sequential circuit

Storage elements are flip-flops

Output value stored in flip-flop when clock occurs

Prior to the occurrence of the clock the combinational output must be stable

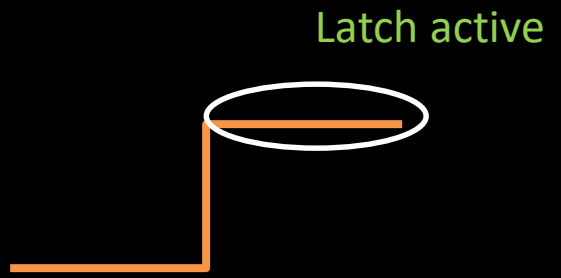
Speed of the combinational logic is critical

Storage elements

Maintains a binary state indefinitely until directed by an input signal to switch states

Latches

Storage elements that operate with signal levels (rather than signal transitions)



Level Sensitive

Flip-Flops

Storage elements that are controlled by clock transitions

Edge Sensitive

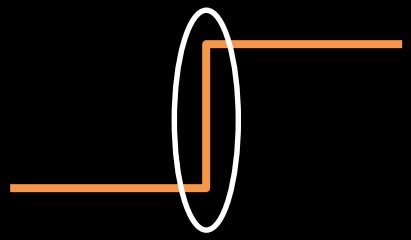
Storage elements

Maintains a binary state indefinitely until directed by an input signal to switch states

Latches

Storage elements that operate with signal levels (rather than signal transitions)

Level Sensitive

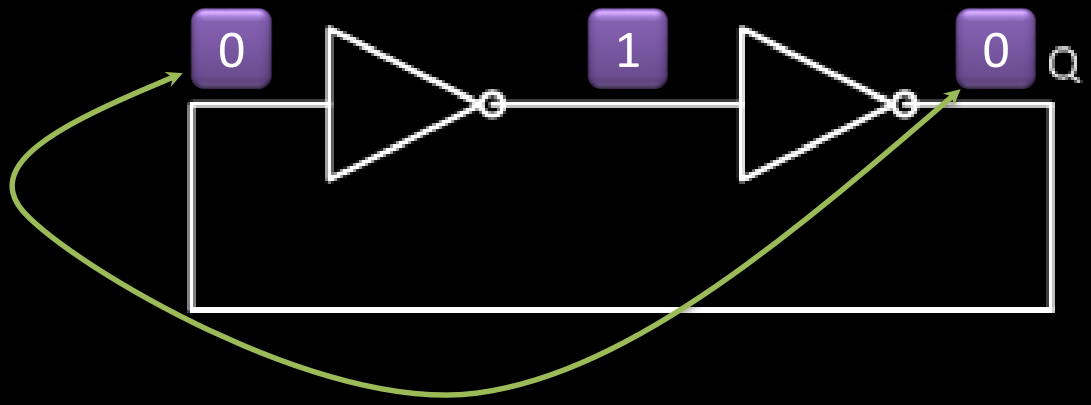


Flip-Flops

Storage elements that are controlled by clock transitions

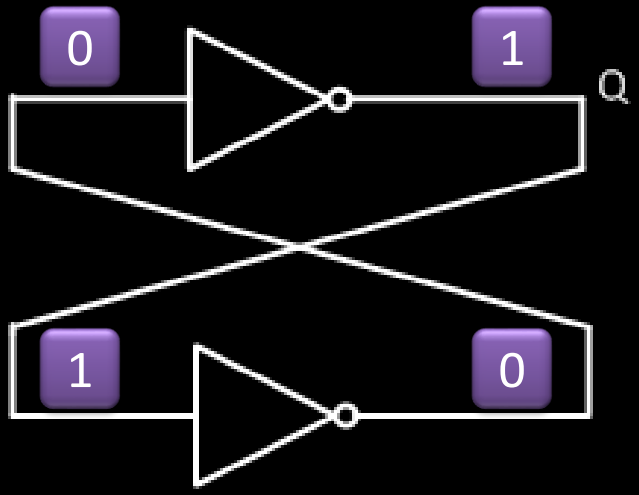
Edge Sensitive

Storage elements



Storing 0

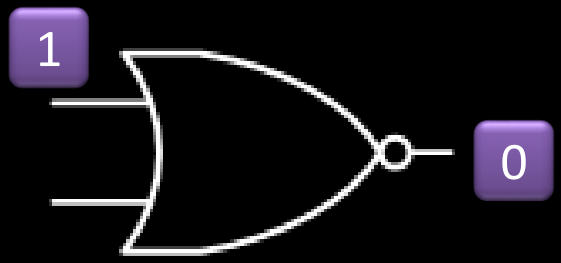
Storage elements

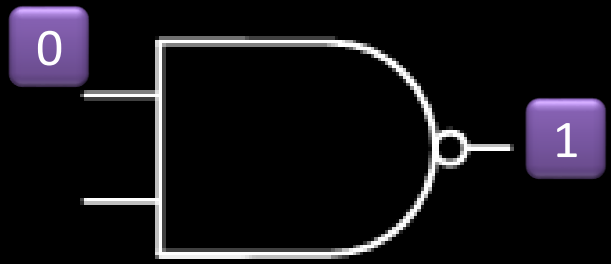


Storing 0

Is there any way to control the storage value ?

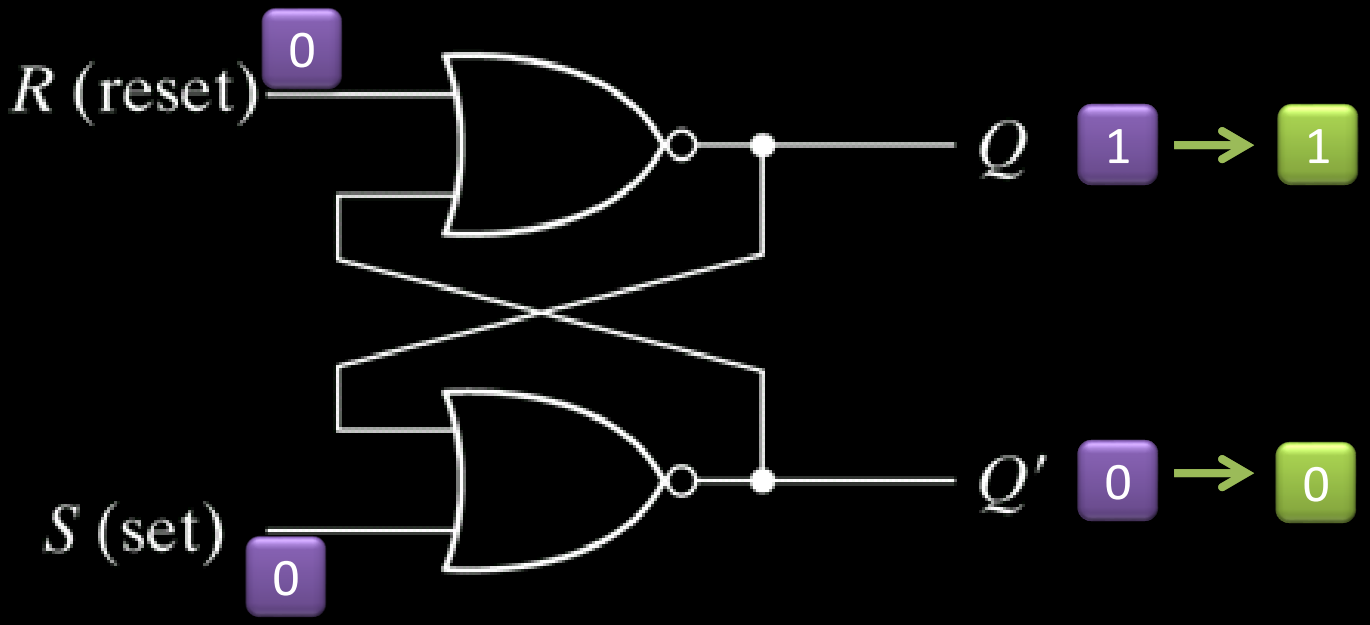
NOR -NAND





Latches

SR Latch

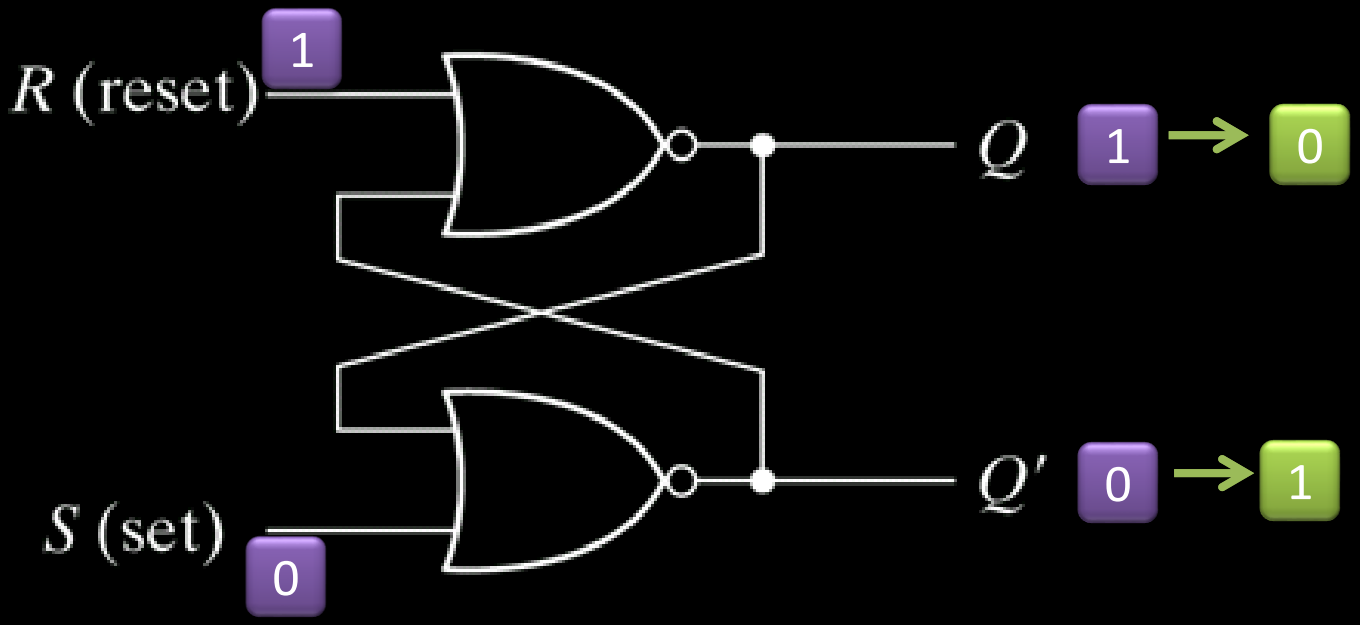


Reset = 0, Set = 0 No change in outputs

New state = Old state

Latches

SR Latch

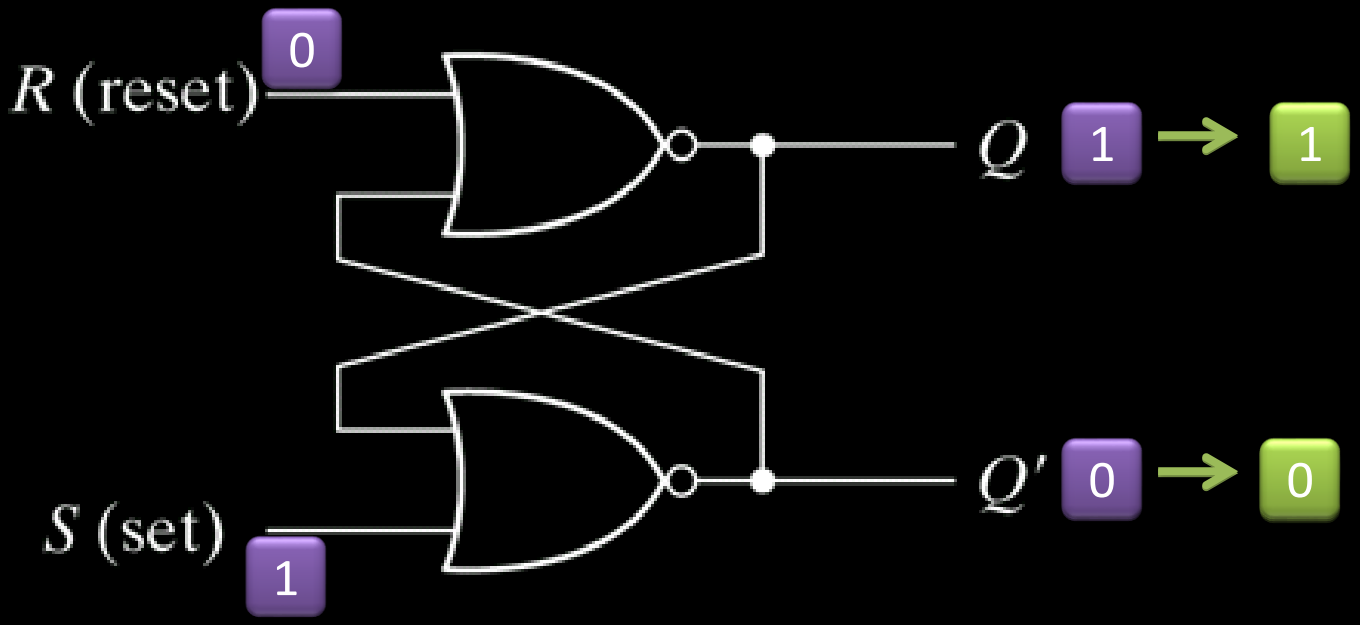


Reset = 1, Set = 0 Q = 0 and Q' = 1

Reset operation

Latches

SR Latch

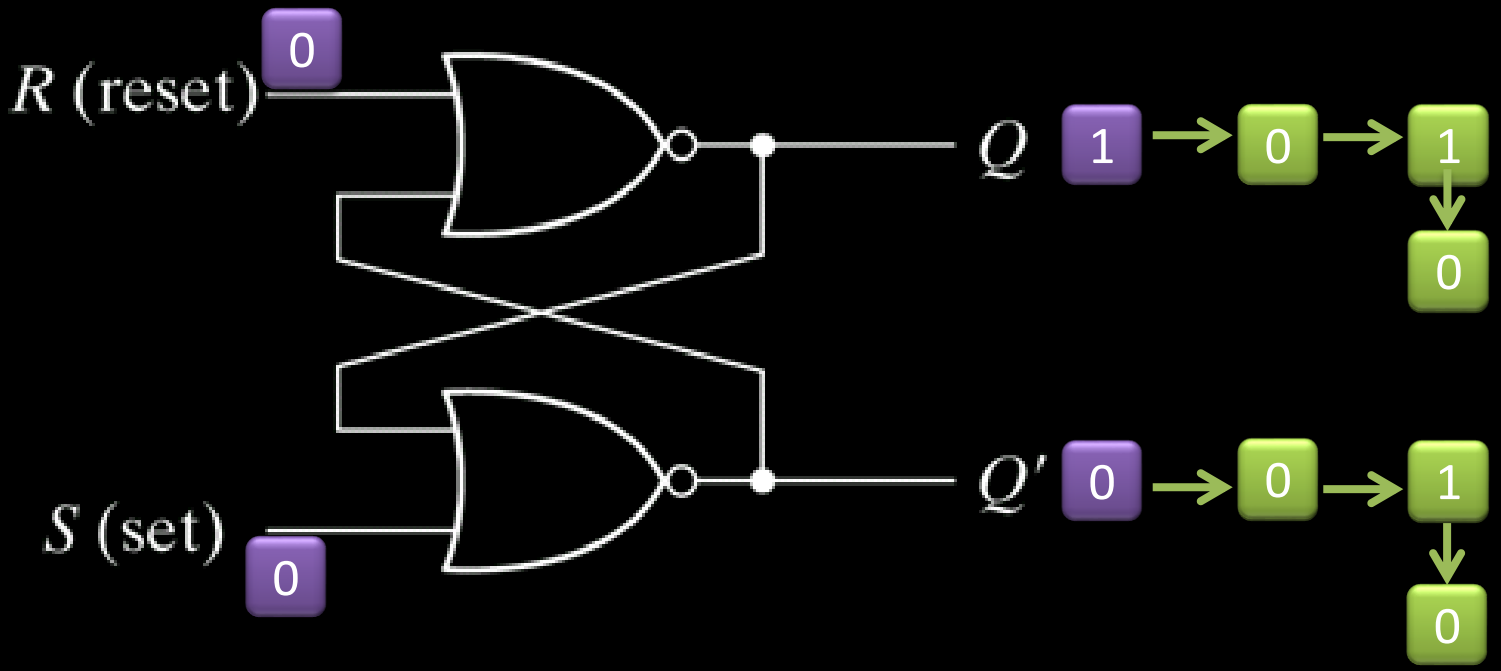


Reset = 0, Set = 1 Q = 1 and Q' = 0

Set operation

Latches

SR Latch



Reset = 1, Set = 1 Q = 0 and Q' = 0 But

Reset = 0, Set = 0

Cant predict output - > metastable state

Latches

SR Latch

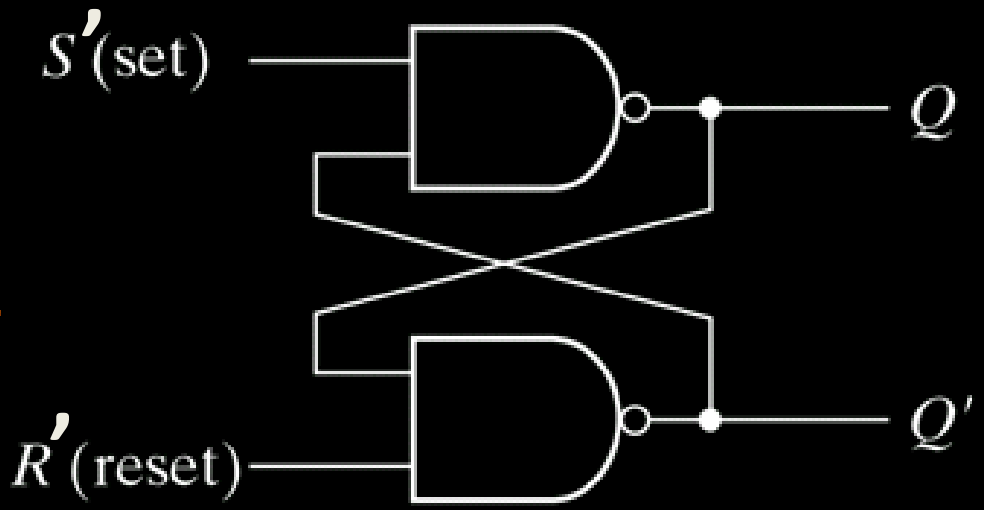
Cant predict output - > metastable state

Set = 1, reset = 1 is thus forbidden state

S	R	Q	Q’	
0	0	Q	Q’	No change
0	1	0	1	Reset
1	0	1	0	set
1	1	0	0	Forbidden

Latches

S'R' Latch



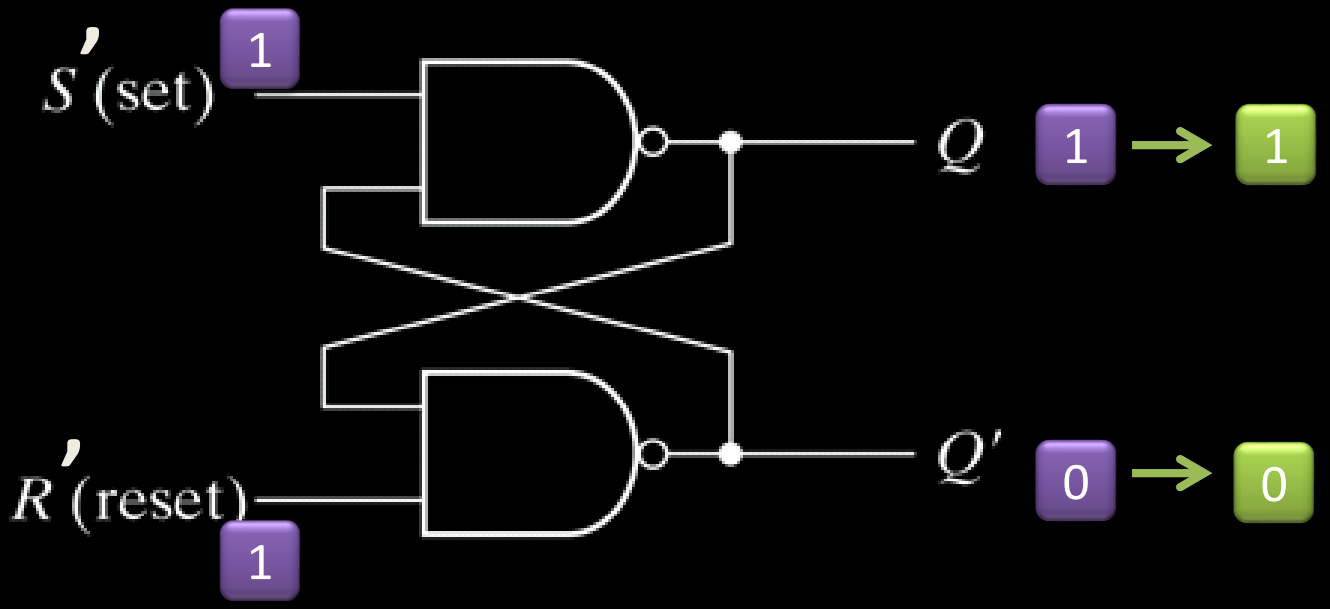
Latches

S'R' Latch

S	R	Q	Q'	
0	0	1	1	Forbidden
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q	Q'	No change

Latches

S'R' Latch

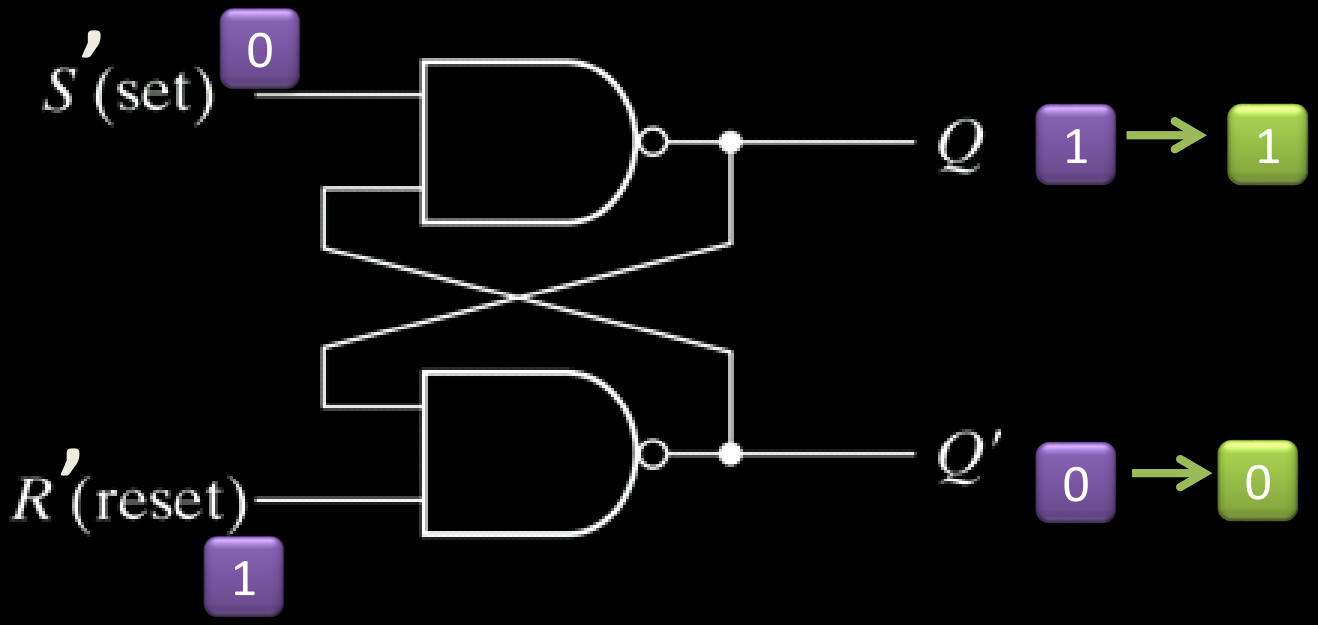


Reset' = 1, Set' = 1 No change in outputs

New state = Old state

Latches

S'R' Latch

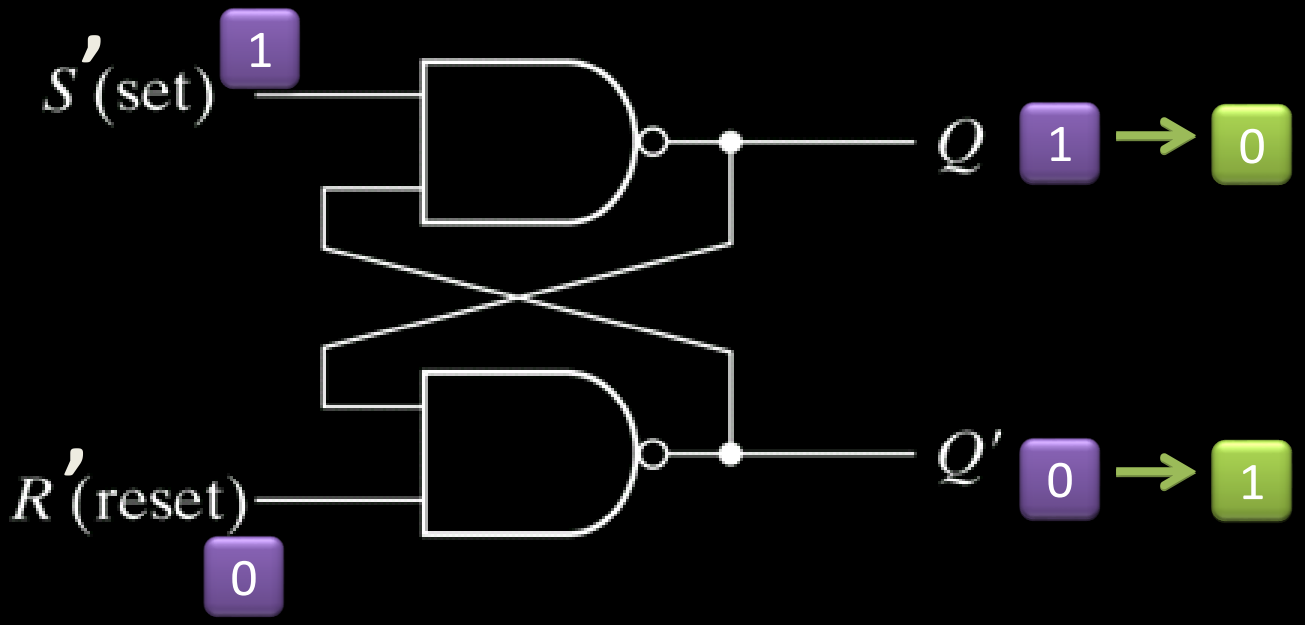


Reset' = 1, Set' = 0 Q = 1 and Q' = 0

set operation

Latches

SR Latch

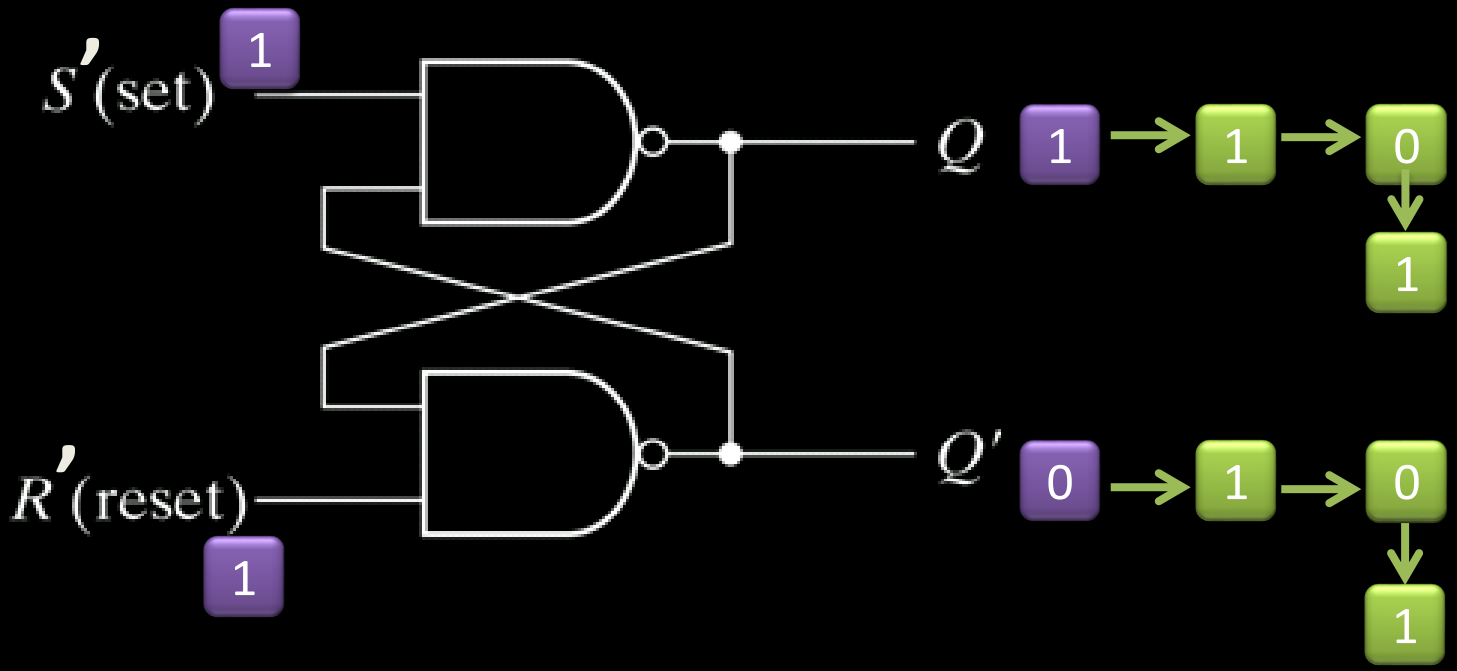


Reset' = 0, Set' = 1 Q = 0 and Q' = 1

Reset operation

Latches

SR Latch



Reset' = 0, Set' = 0 Q = 1 and Q' = 1 But

Reset' = 1, Set' = 1

Cant predict output - > metastable state

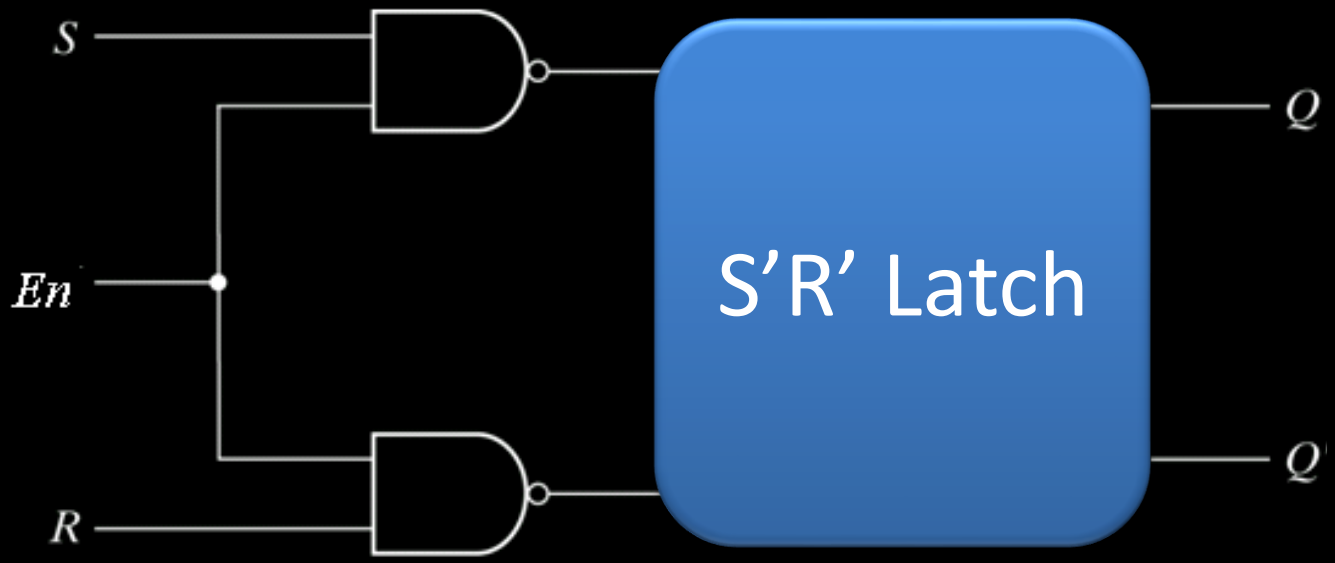
Latches

S'R' Latch

S	R	Q	Q'	
0	0	1	1	Forbidden
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q	Q'	No change

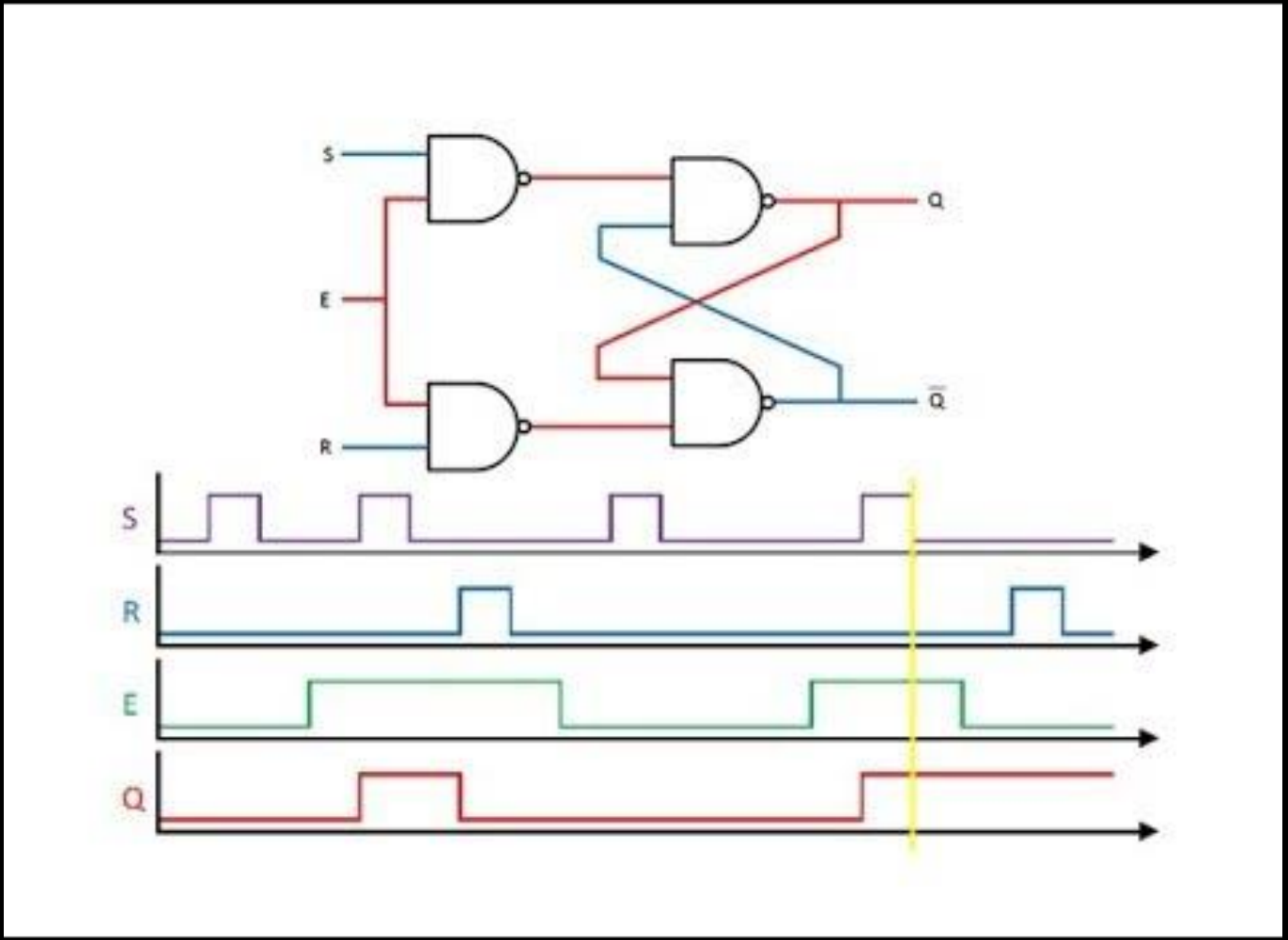
Latches

SR Latch with enable



Latches

SR Latch with enable



Thank You