

Digital Electronics and Computer Organization

Digital Design

Lecture 12: 4 Bit Adders , Multipliers and Magnitude Comparators



Birla Institute of Technology & Science, Pilani
Hyderabad Campus

Innovate

achieve

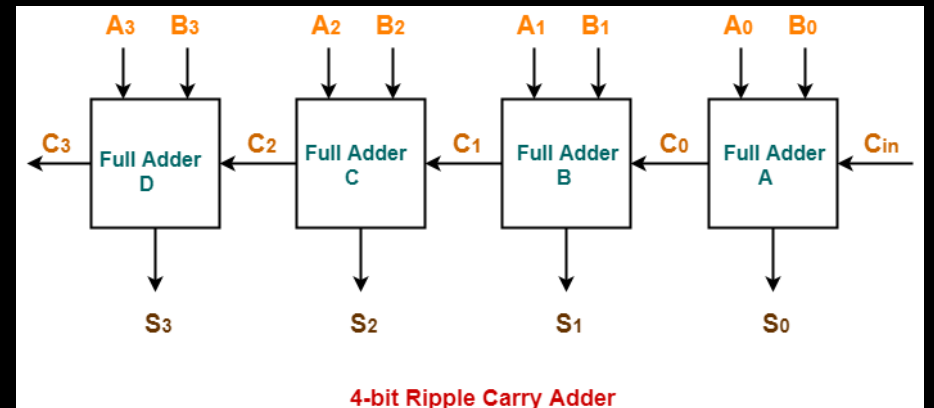
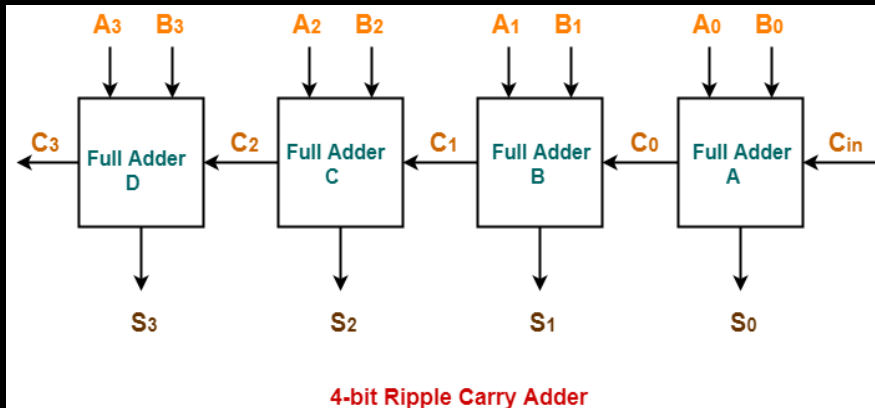
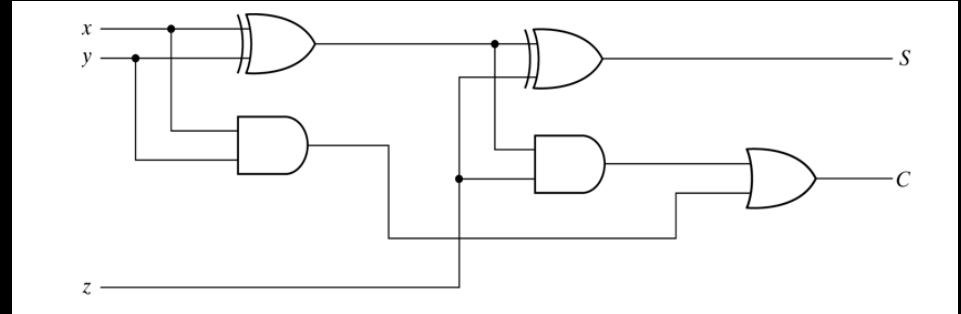
1

lead



Ripple Carry Adder

8 Bit Full Adder

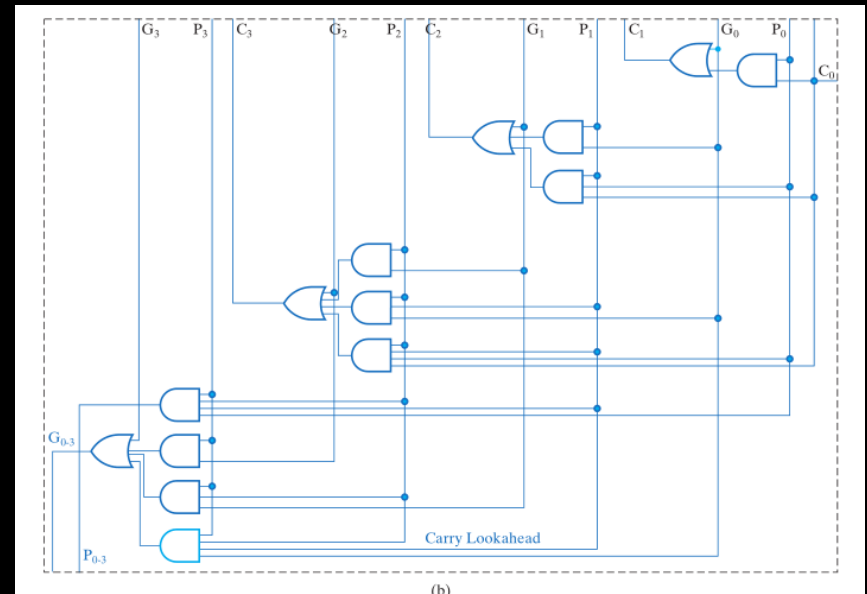
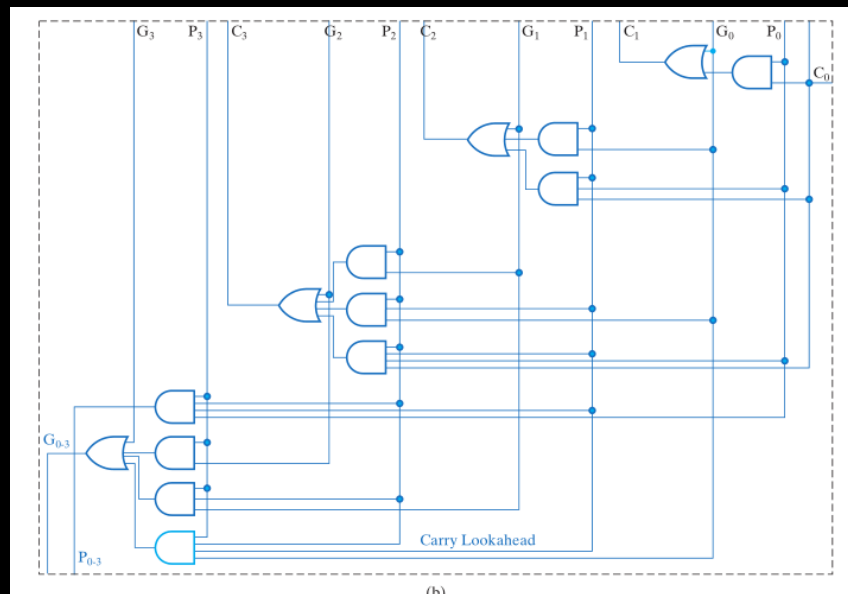
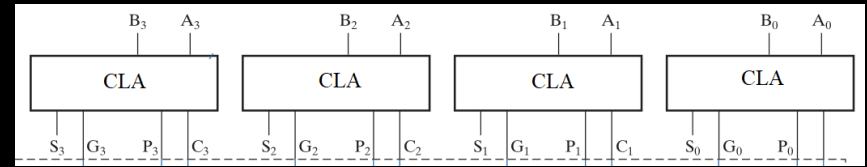
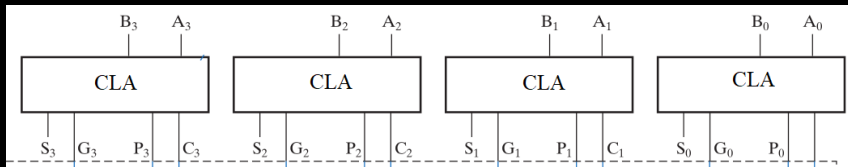


Delay = 8 X 3 Gate Delay



Carry Look-Ahead Adder

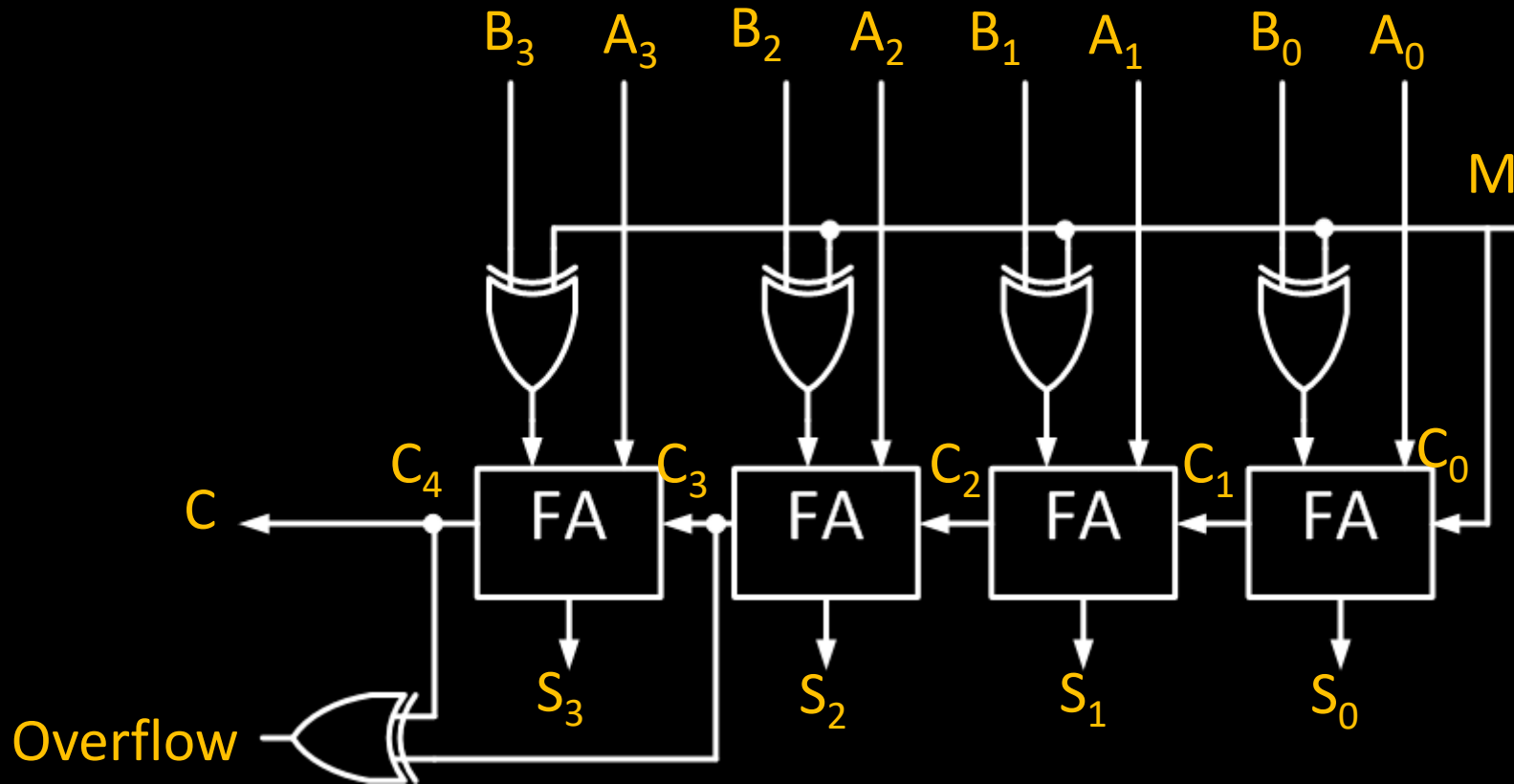
8 Bit Full Adder



Delay = 2 X 3 Delay



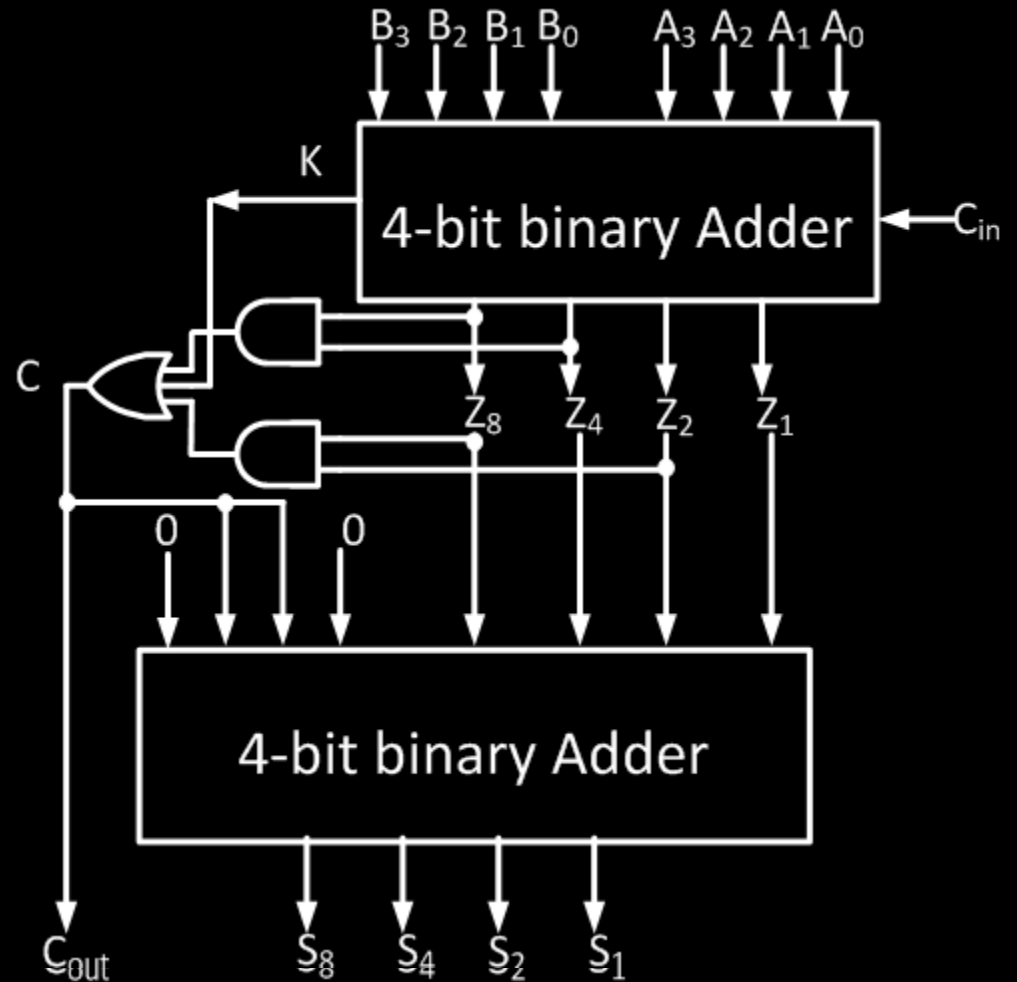
4-bit Adder subtractor with overflow detection





BCD Adder

If C is 1 Add 6
If C is 0 Add 0





Binary Multiplier

$$\begin{array}{r} 23 \\ \times 52 \\ \hline \end{array}$$



Binary Multiplier

2 3

$$\begin{array}{r} \times \quad 5 \quad 2 \\ \hline \quad 4 \quad 6 \end{array}$$

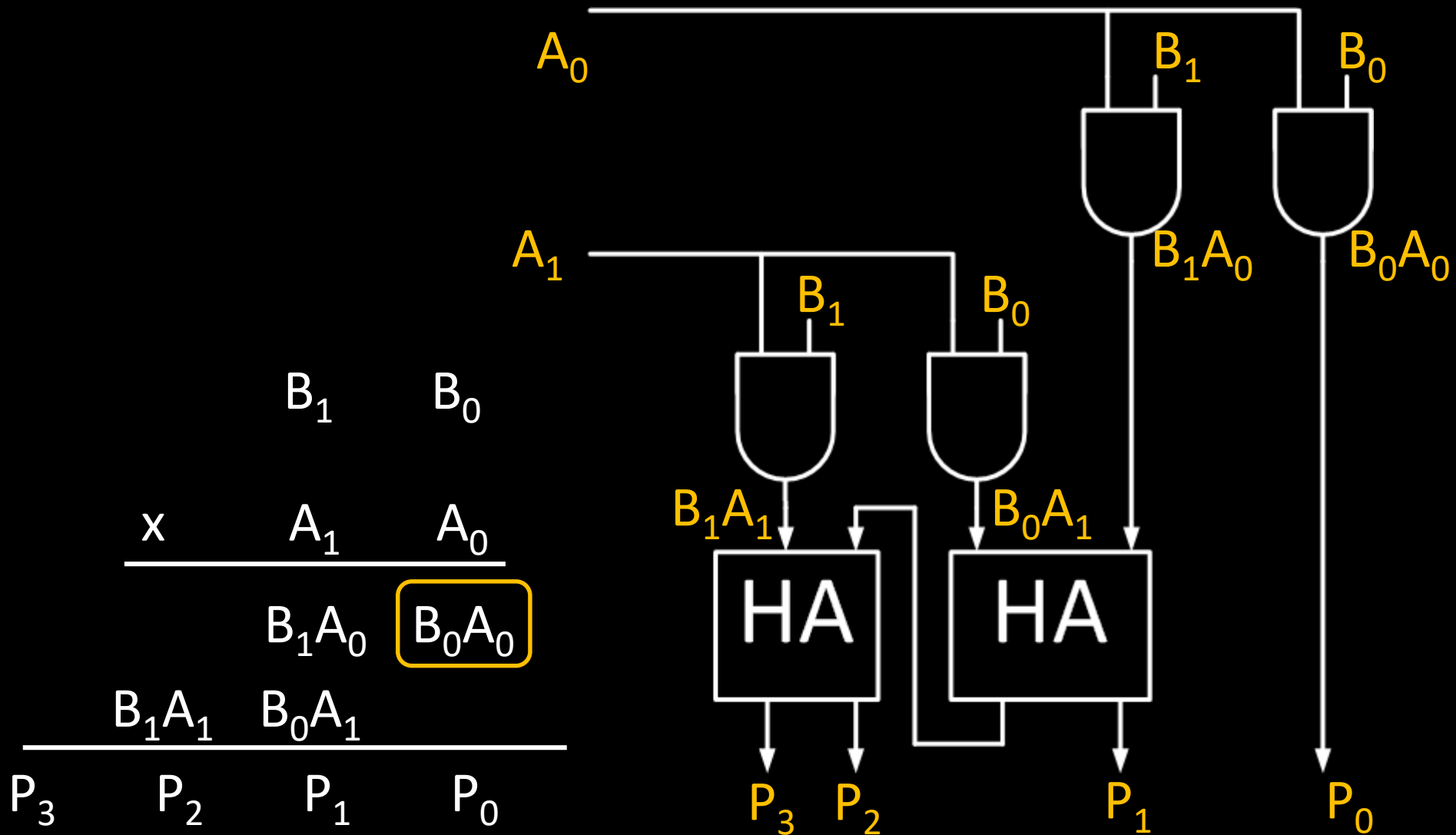
$$\begin{array}{r} 1 \quad 1 \quad 5 \\ \hline 1 \quad 1 \quad 9 \quad 6 \end{array}$$

1 0

$$\begin{array}{r} \times \quad 1 \quad 1 \\ \hline \end{array}$$



Binary Multiplier





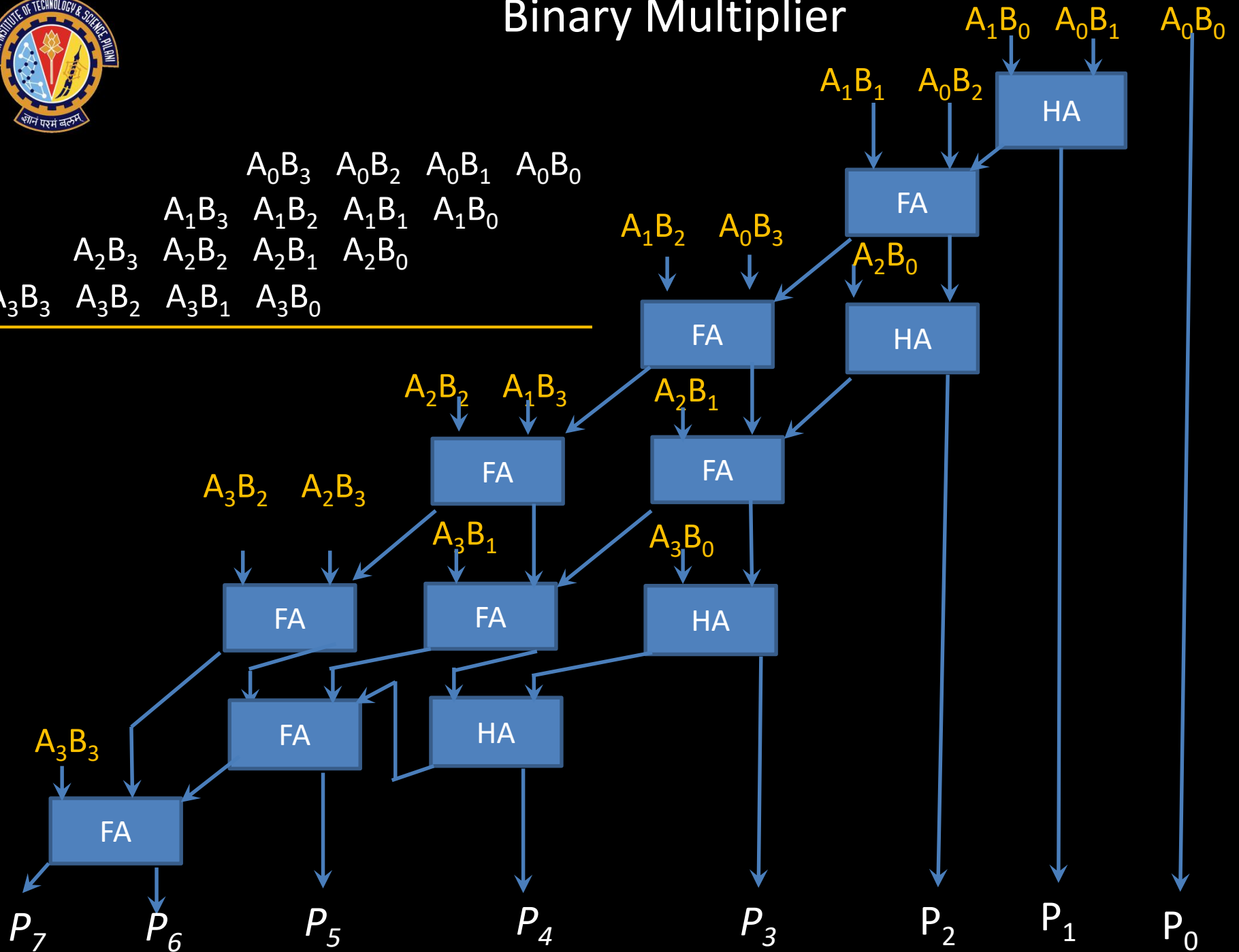
Binary Multiplier

$$\begin{array}{r} \text{(Multiplicand)} \quad B_3 \quad B_2 \quad B_1 \quad B_0 \\ \text{(Multiplier)} \quad \quad A_3 \quad A_2 \quad A_1 \quad A_0 \\ \hline A_0 B_3 \quad A_0 B_2 \quad A_0 B_1 \quad A_0 B_0 \\ A_1 B_3 \quad A_1 B_2 \quad A_1 B_1 \quad A_1 B_0 \\ A_2 B_3 \quad A_2 B_2 \quad A_2 B_1 \quad A_2 B_0 \\ A_3 B_3 \quad A_3 B_2 \quad A_3 B_1 \quad A_3 B_0 \\ \hline \end{array}$$



Binary Multiplier

		A_0B_3	A_0B_2	A_0B_1	A_0B_0
	A_1B_3	A_1B_2	A_1B_1	A_1B_0	
A_2B_3	A_2B_2	A_2B_1	A_2B_0		
A_3B_3	A_3B_2	A_3B_1	A_3B_0		





Magnitude Comparator

A Magnitude comparator is a **combinational circuit that compares two numbers A and B**.

The output of the magnitude comparator are three signals that indicate if **$(A > B)$, $(A < B)$, $(A = B)$**

Even a 3-bit comparator results in 6 inputs – Too complex to solve using K-maps

Look for Regularity in design



Magnitude Comparator

How do you compare two numbers?

2	3	4
5	6	4

Compare most significant digit

If most significant digit of first number is greater than the most significant digit of second number then

First Number > Second number



Magnitude Comparator

If most significant digits are equal ??

2	3	4
2	6	4

Compare the next significant digit

If next significant digit of first number is greater than the next significant digit of second number then

First Number > Second number

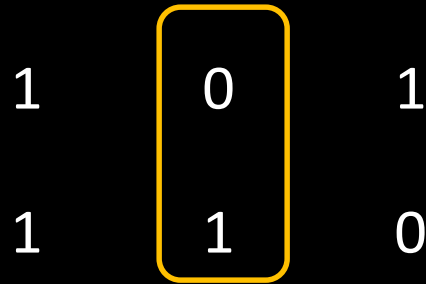


Magnitude Comparator

1	0	1
1	1	0



Magnitude Comparator





Magnitude Comparator

1-Bit Comparator

A_0

B_0

Let G_0 indicate greater, L_0 indicate Lesser and E_0 indicate equal

A_0	B_0	G_0	L_0	E_0
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

$$G_0 = A_0 B_0'$$

$$L_0 = A_0' B_0$$

$$E_0 = (A_0 \oplus B_0)' = (A_0 \odot B_0) = (G_0 + L_0)'$$

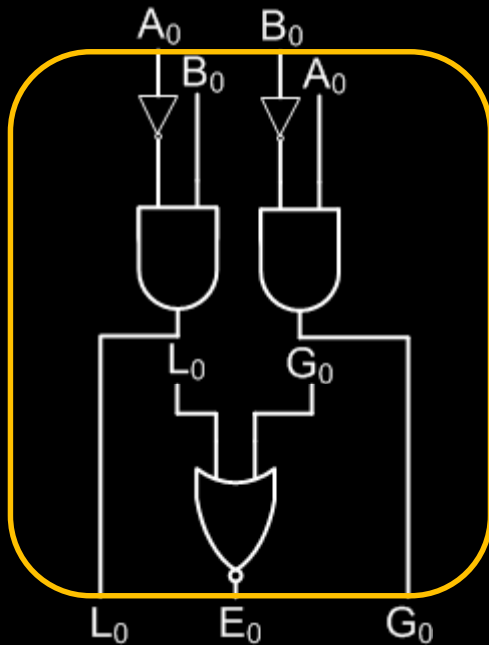


Magnitude Comparator

1-Bit Comparator

A_0

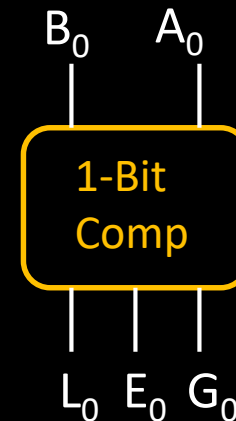
B_0



$$G_0 = A_0 B_0'$$

$$L_0 = A_0' B_0$$

$$E_0 = (G_0 + L_0)' = (A_0 \oplus B_0)'$$





Magnitude Comparator

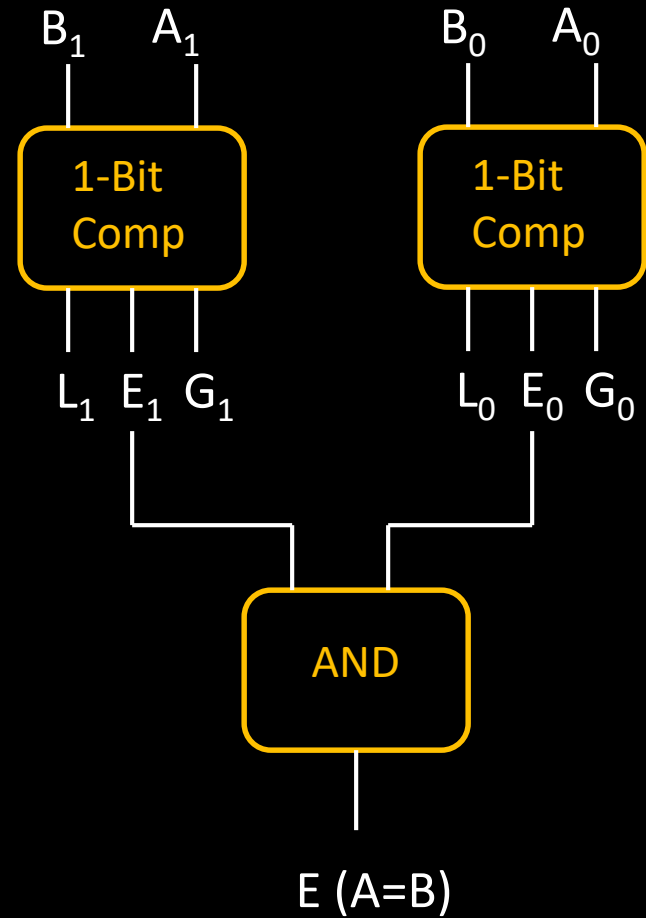
2-Bit Comparator

A $A_1 A_0$

B $B_1 B_0$

A = B When $A_0 = B_0$ and $A_1 = B_1$

$$E = E_0 \cdot E_1$$





Magnitude Comparator

2-Bit Comparator

A $A_1 A_0$

B $B_1 B_0$



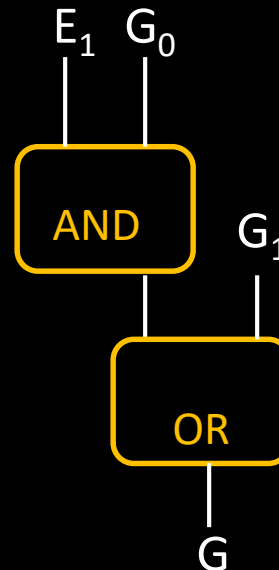
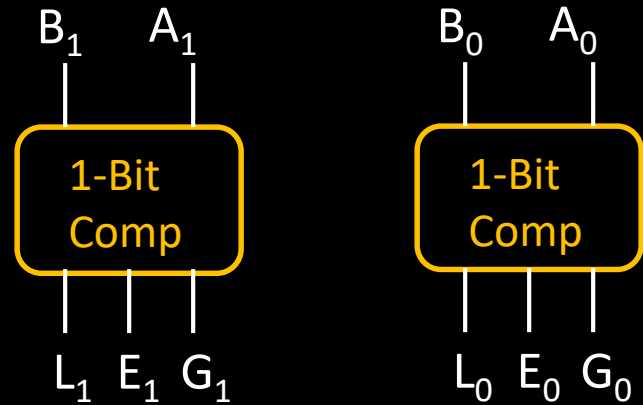
Magnitude Comparator

2-Bit Comparator

A $A_1 A_0$
 B $B_1 B_0$

$A > B$ When $A_1 > B_1$ **OR**
 When $A_1 = B_1$ and $A_0 > B_0$

$$G = G_1 + E_1 \cdot G_0$$





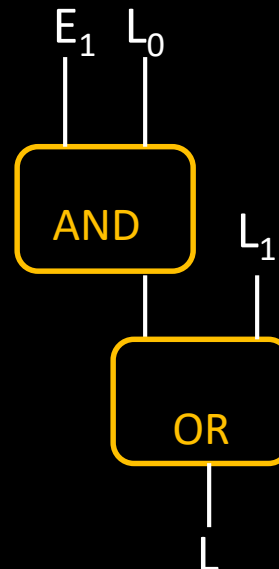
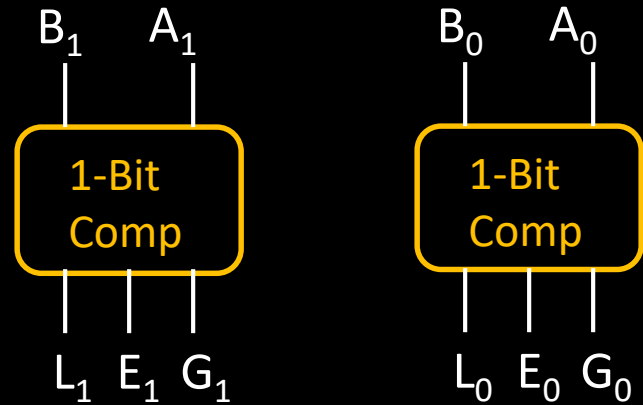
Magnitude Comparator

2-Bit Comparator

A $A_1 A_0$
B $B_1 B_0$

$A < B$ When $A_1 < B_1$ **OR**
 When $A_1 = B_1$ and $A_0 < B_0$

$$L = L_1 + E_1 \cdot L_0$$





Magnitude Comparator

1-Bit Comparator

$$G = G_0 \quad L = L_0 \quad E = E_0$$

2-Bit Comparator

$$G = G_1 + E_1 \cdot G_0 \quad L = L_1 + E_1 \cdot L_0 \quad E = E_1 \cdot E_0$$

3-Bit Comparator

$$G = G_2 + E_2 \cdot G_1 + E_2 \cdot E_1 \cdot G_0$$

$$E = E_2 \cdot E_1 \cdot E_0$$

$$L = L_2 + E_2 \cdot L_1 + E_2 \cdot E_1 \cdot L_0$$



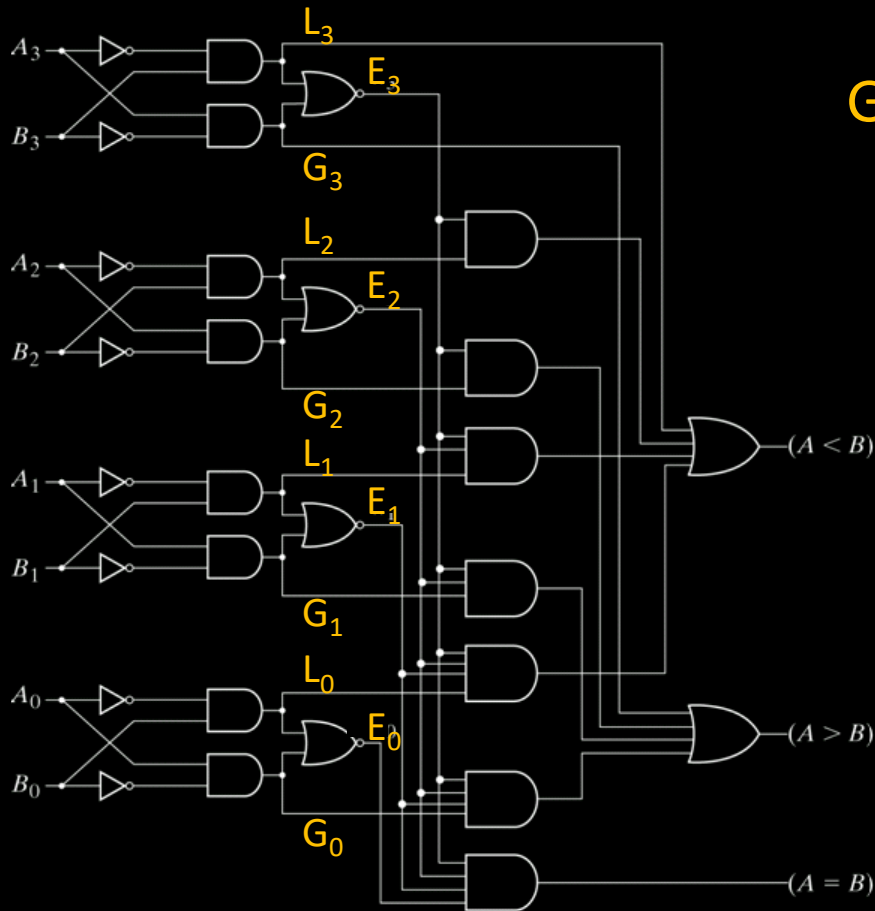
Magnitude Comparator

4-Bit Comparator

$$G = G_3 + E_3 \cdot G_2 + E_3 \cdot E_2 \cdot G_1 + E_3 \cdot E_2 \cdot E_1 \cdot G_0$$

$$L = L_3 + E_3 \cdot L_2 + E_3 \cdot E_2 \cdot L_1 + E_3 \cdot E_2 \cdot E_1 \cdot L_0$$

$$E = E_2 \cdot E_1 \cdot E_0$$



Can you draw the circuit ??



Next Module

Decoders

Encoders

Multiplexers



Thank You