OVERVIEW

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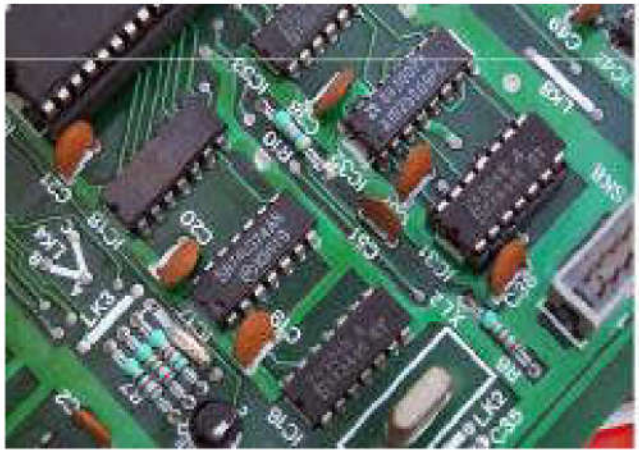
- Transistor as a Switch
- RTL, DTL, TTL and ECL
- Elementary data of CMOS



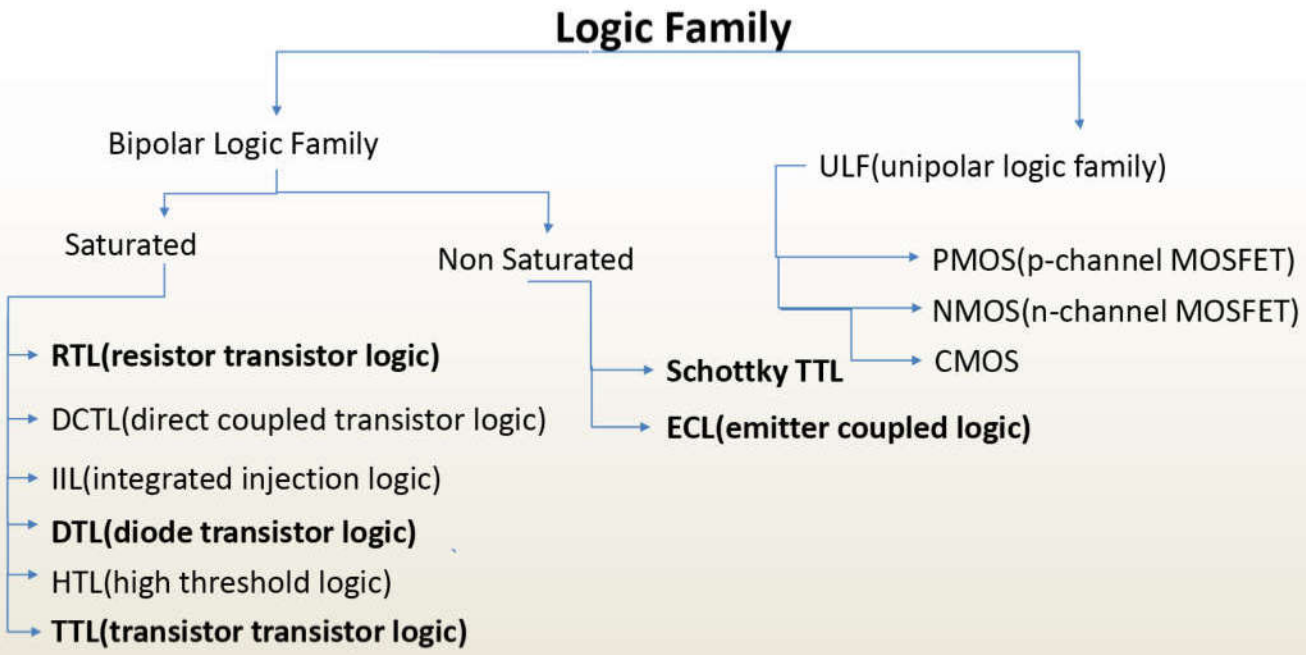
Introduction

Logic families represent kind of digital circuit/methodologies for logic expression.

Integration levels :

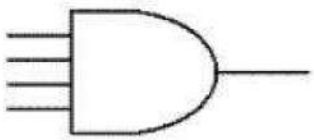
SSI: Small scale integration	**12 gates/chip**
MSI: Medium scale integration	**100 gates/chip**
LSI: Large scale integration	**1K gates/chip**
VLSI: Very large scale integration	**10K gates/chip**
ULSI: Ultra large scale integration	**100K gates/chip**

Classification



Fan In

- Fan in or gate is the number of inputs that can practically be supported without degrading practically input voltage level.



Fan in = 4

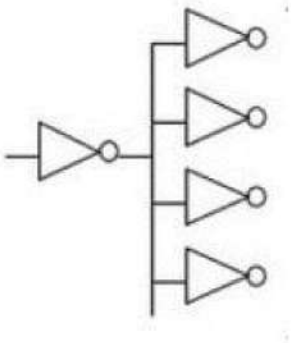
Fan Out

•The maximum number of digital input that the output of a single logic gate can feed and the gate must be same logic family.

• Fan Out is calculated from the amount of current available in the output of a gate and the amount of current needed in each input of the connecting gate.

•It is specified by manufacturer and is provided in the data sheet.

•Exceeding the specified maximum load may cause a malfunction because the circuit will not be able supply the demanded power.



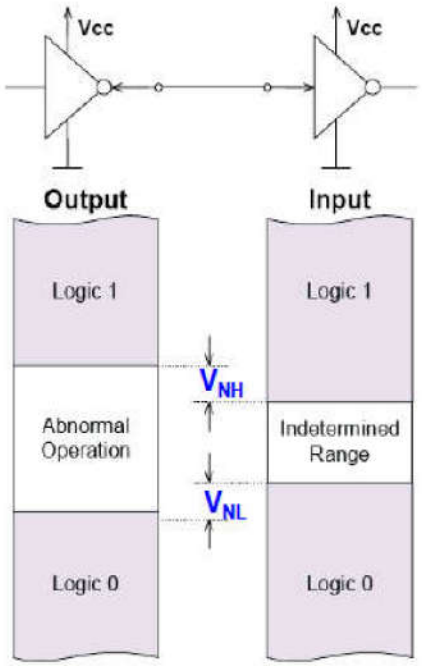
Fanout = 4

Noise Margin

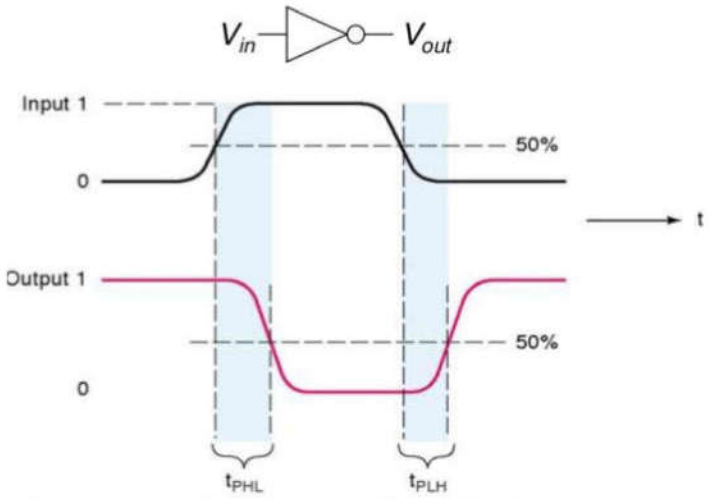
•Noise is present in all real systems. This adds random fluctuations to voltages representing logic levels.

•Hence, the voltage ranges defining the logic levels are more tightly constrained at the output of a gate than at the input.

• Small amounts of noise will not affect the circuit. The maximum noise voltage that can be tolerated by a circuit is termed its **noise immunity (noise Margin).**



Propagation Delay



A measure of how long it takes for a gate to change state. Ideally, should be as short as possible.

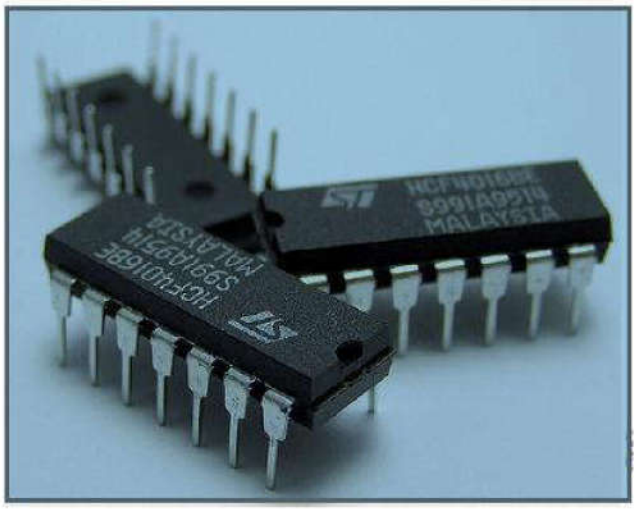
t_{PHL} - the time it takes the output to go from a high to a low

t_{PLH} - the time it takes the output to go from a low to a high

Average Propagation Delay Time $t_p = \frac{t_{pHL} + t_{pLH}}{2}$

Basic Characteristics of ICs

- Propagation delay
- Power dissipation
- Fan in and fan out
- Noise immunity
- Power supply requirement
- Figure of merits i.e. speed power product
- Operating temperature
- Current and voltage parameters

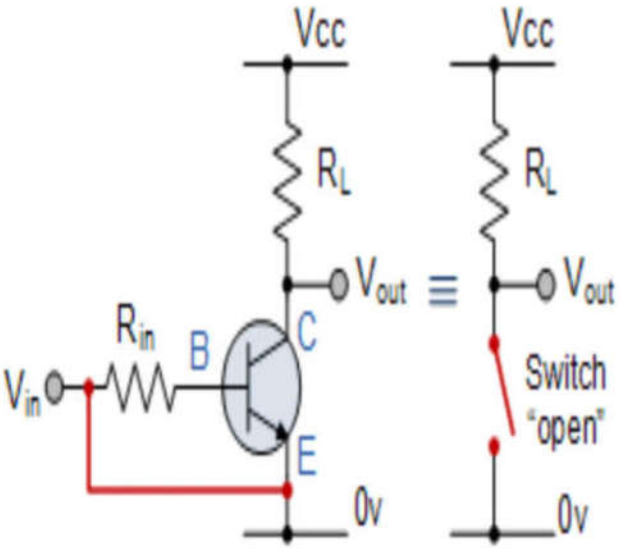


Transistor as a switch

- A circuit that can turn on/off current in electrical circuit is referred to a switching circuit and transistor can be employed as an electronic switch.

- Cut off region - OFF State
  Both junctions are reverse biased,
  Ic = 0 and V(BE) < 0.7 v

- Saturation region - ON State
  Ic = maximum and V(BE)>0.7 v



Resistor Transistor Logic(RTL)

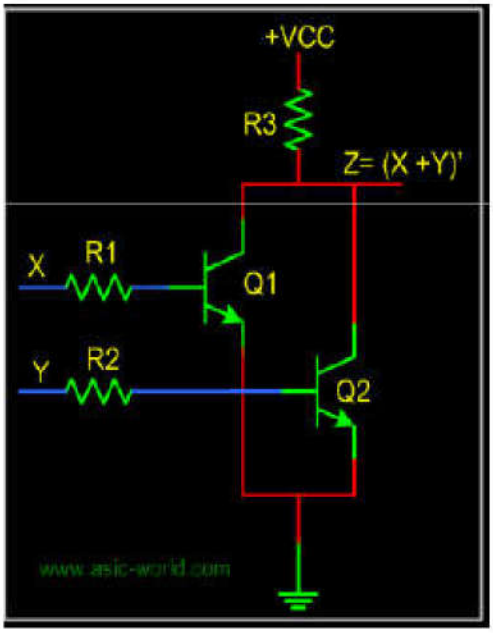
- The basic RTL device is a NOR gate.
- The inputs represent either logic level HIGH (1) or LOW (0).
- The logic level LOW is the voltage that drives corresponding transistor in cut-off region, while logic level HIGH drives it into saturation region.
- If both the inputs are LOW, then both the transistors are in cut-off i.e. they are turned-off. Thus, voltage Vcc appears at output I.e. HIGH.
- If either transistor or both of them are applied HIGH input, the voltage Vcc drops across Rc and output is LOW.

Advantages of RTL Logic circuit:

The primary advantage of RTL technology was that it involved a minimum number of transistors, which was an important consideration before integrated circuit technology, as transistors were the most expensive component to produce

Limitations:

The obvious disadvantage of RTL is its high current dissipation when the transistor conducts to overdrive the output biasing resistor. This requires that more current be supplied to and heat be removed from RTL circuits. In contrast, TTL circuits minimize both of these requirements:



(NOR GATE USING RTL)

Diode Transistor Logic

- The diode-transistor logic, also termed as DTL, replaced RTL family because of greater fan-out capability and more noise margin.
- DTL circuits mainly consists of diodes and transistors that comprises DTL devices.
- The basic DTL device is a NAND gate.
- Two inputs to the gate are applied through diodes viz. D1, D2 . The diode will conduct only when corresponding input is LOW.
- If any of the diode is conducting i.e. when at least one input is LOW, the voltage at output keeps transistor T in cut-off and subsequently, output of transistor is HIGH. If all inputs are HIGH, all diodes are non-conducting, transistor T is in saturation, and its output is LOW.

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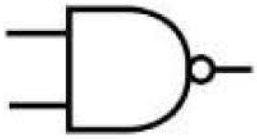
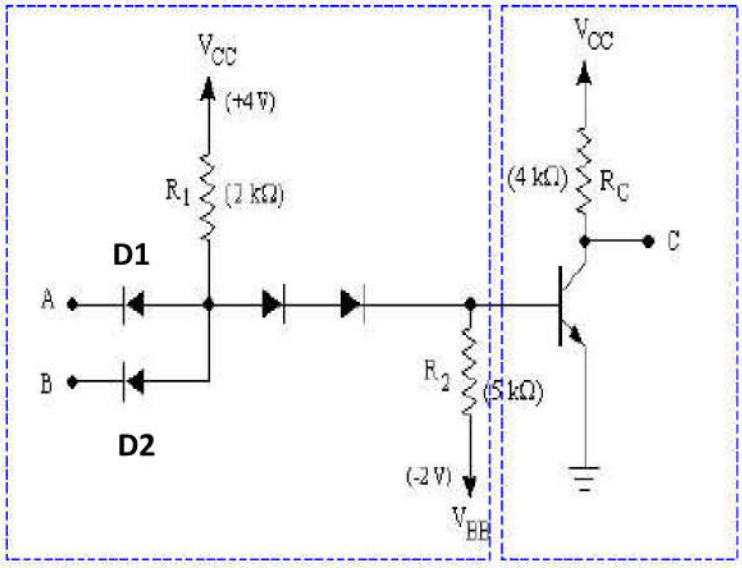
Due to number of diodes used in this circuit, the speed of the circuit is significantly low. Hence this family of logic gates is modified to transistor-transistor logic i.e. TTL family which has been discussed on next slide.





(DL AND GATE) **(SATURATING INVERTER)**

Transistor Transistor Logic

- TTL family is a modification to the DTL. It has come to existence so as to overcome the speed limitations of DTL family. The basic gate of this family is TTL NAND gate.

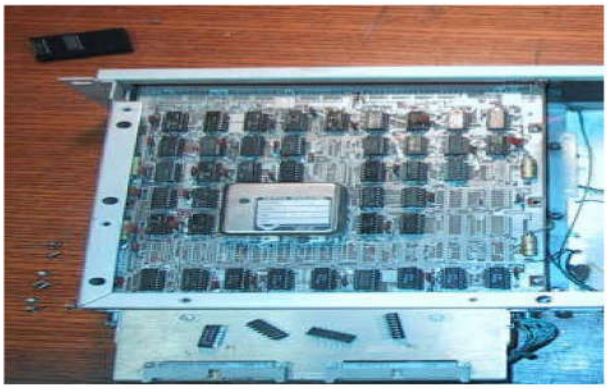
- Q3 is cutoff (act like a high RC) when output transistor Q4 is saturated and Q3 is saturated (act like a low RC) when output transistor Q4 is cutoff . Thus one transistor is ON at one time.

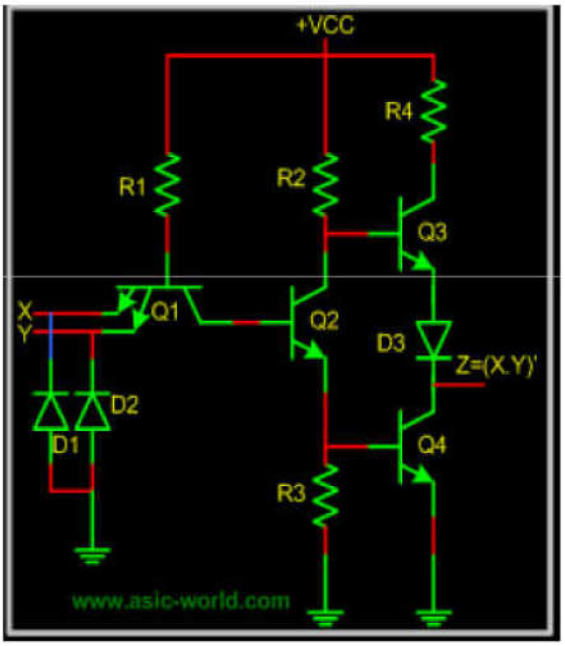
- The combination of Q3 and Q4 is called TOTEM POLE arrangement.

- Q1 is called input transistor, which is multi emitter transistor, that drive transistor Q2 which is used to control Q3 and Q4.

- Diode D1 and D2 are used to protect Q1 from unwanted negative voltages and diode D3 ensures when Q4 is ON, Q3 is OFF.

The output impedance is asymmetrical between the high and low state, making them unsuitable for driving transmission lines. This drawback is usually overcome by buffering the outputs with special line-driver devices where signals need to be sent through cables. ECL, by virtue of its symmetric low-impedance output structure, does not have this drawback.





(BLOCK DIAGRAM OF TTL)

Emitter Coupled Logic

- ECL logic family implements the gates in differential amplifier configuration in which transistors are never driven in the saturation region thereby improving the speed of circuit to a great extent. The ECL family is fastest of all logic families.

- Based on BJT, but removes problems of delay time by preventing the transistors from saturating.

- Very fast operation - propagation delays of 1ns or less.

- Low noise immunity of about 0.2-0.25 V .

- The input impedance is high and the output impedance is low. As a result, the transistors change states quickly, gate delays are low, and the fan out capability is high.

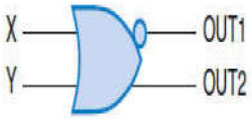
(FUNCTION TABLE)

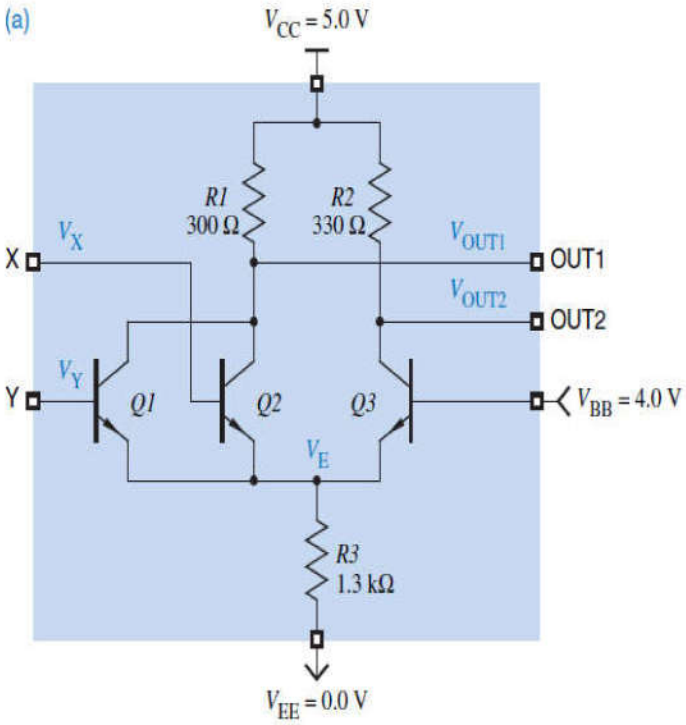
X	Y	V_X	V_Y	*Q1*	*Q2*	*Q3*	V_E	V_{OUT1}	V_{OUT2}	OUT1	OUT2
L	L	3.6	3.6	OFF	OFF	on	3.4	5.0	4.2	H	L
L	H	3.6	4.4	OFF	on	OFF	3.8	4.2	5.0	L	H
H	L	4.4	3.6	on	OFF	OFF	3.8	4.2	5.0	L	H
H	H	4.4	4.4	on	on	OFF	3.8	4.2	5.0	L	H

(TRUTH TABLE)

X	Y	OUT1	OUT2
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

(LOGIC SYMBOL)





(ECL 2 INPUT OR/NOR GATE)

Complimentary MOS (CMOS)

- Considerably lower energy consumption than TTL and ECL, which has made portable electronics possible.
- Most widely used family for large-scale devices
- Combines high speed with low power consumption
- Usually operates from a single supply of 5 – 15 V
- Excellent noise immunity of about 30% of supply voltage
- Can be connected to a large number of gates (about 50) .

Some statistical characteristics data of different logic families

S.N.	Parameter	DTL	HTL	TTL	RTL	ECL	MOS	CMOS
1.	Basic Gates (Positive Logic)	NAND	NAND	NAND	NOR	OR-NOR	NAND	NOR or NAND
2.	Fan out (Minimum)	8	10	10	5	24	20	>50
3.	Typical power dissipation per gate, mW	8-12	55	12-22	12	40-55	0.2-10	0.01 static 1 at 3 MHz
4.	Noise immunity	Good	Excellent	Very good	Medium	Good	Medium	Very good
5.	Typical propagation delay/gate, ns	30	90	12-6	12	4-1	300	70
6.	Clock rate (minimum frequency at which flip-flops operate), MHZ	12-30	4	15-60	8	60-400	2	5
7.	Number of functions	Fairy High	Medium	Very high	high	High	Low	Low

References

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- ✓ Logic Families by Dr. Basem Elhalawany
- ✓ Logic Gates and Family by Dr. A. P. VAJPEYI, IITG

Thank You