



# Digital Design : 2020-21 Lab 4 Introduction to Verilog and Implementation of Majority Circuit in Xilinx ISE By Dr. Sanjay Vidhyadharan







(Go to Slide no. 3 for Windows Home Edition)

# For Window Professional

### 1. Download Xilinx\_ISE\_For\_Windows\_Professional\_S6\_Win10\_14.7\_ISE\_VMs\_0206\_1.zip

from <u>http://sanjayvidhyadharan.in/Downloads/</u>

2. Install xsetup.exe







- 1. Download Xilinx\_ISE\_For\_Window\_Home\_DS\_Win\_14.1\_P.15xf.0.1.rar
  - from <u>http://sanjayvidhyadharan.in/Downloads/</u>
- 2. Install xsetup.exe



3. Make the following choices during installation process





3. Make the following specific choices during installation process (Most of them are default and not shown below. Only Variations that are to be done are highlighted below:-)







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3. Make the following specific choices during installation process (Most of them are default and not shown below. Only Variations that are to be done are highlighted below:-)





## **Gate Level Modelling**

Simple Circuit to demonstrate HDL





## **Simple Circuit for Demonstration**



module Simple\_circuit (input A, input B, input C, output x, output y); wire w1;

and g1 (w1,A,B); // and gate instance not g2 (y,C); or g3 (x,w1,y);

endmodule



## **Problem Definition**

- 1. Three-bit Majority Circuit
- 2. Parity Encoder

Additional Problems for Practice → Gray to Binary code

### ELECTRICAL ELECTRONICS COMMUNICATION INSTRUMENTATION

#### Learning Objectives

(1) Implement and verify the following modules using Verilog gate level modelling

3-input majority function using AND - OR gates

(2) Implementing the Verilog designs on to FPGA

**Exercise 1:** Design and Implementation of simplified SOP form of a Boolean <u>3-input majority</u> function using AND – OR gates

**Design & Implementation for simplified SOP form of Majority Function:** A three-input majority circuit having A(MSB), B and C(LSB) as inputs with output F is shown in the figure below.



Figure 3.1 : Three-input Majority Circuit

### STEPS FOR IMPLEMENTING THE VERILOG CODE

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Write Verilog code for gate-level design of Majority Function using logic gates. In this design you require three 2-input AND gates and two 2-input OR gates.

### Partial Verilog Code for Majority Function: major\_func.v

module major\_func ( Input A, Input B, Input C, Output F ); Wire w1, w2, w3, w4; and g1(w1, A, B); // AND gate instance for g1 // with A & B are as inputs and w1 as output.

// similarly write the AND gate instances
// for g2 & g4

//w1 & w2 are now inputs to OR gate g3.
or g3(w3, w1, w2);

// similarly write the OR gate instance for g5.

endmodule

#### STEPS FOR TESTING THE VERILOG CODE

For testing make sure the view is selected as Simulation

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Check the syntax of the Verilog code by double clicking on <u>Behavioral Check syntax</u> in the Process window (Under ISim Simulator).



After the syntax is checked simulate your Verilog code by double clicking on <u>Simulate</u> Behavioral Model. (Under ISim Simulator)



A simulation window will open.



Here you have to give different patterns to inputs by right clicking on the input select <u>"Force</u> <u>Constant"</u>.



Specify the value of the input. Then Click on Ok.

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Repeat this for all inputs and then click  $\mathbf{k}^{\mathbf{X}}$  to run the simulation for specified amount of time.

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You can test your design by 8 input combinations below. Also follow these steps



Step1: : After forcing the input 000, click  ${}^{>\!\!X}$  button to run for 1us specified on the tool bar, then you can see output F getting updated in the Value column to "0".

Step2: For  $2^{nd}$  combination, just change C to "1" and click to run for next step of 1us, you will notice output remains same.

Step3: Repeat for 3 - 8 combinations and click <sup>20</sup>Zoom to Full View button to see the final <u>Expected Output.</u>

