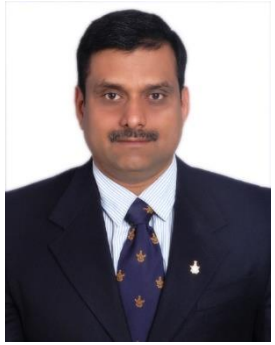
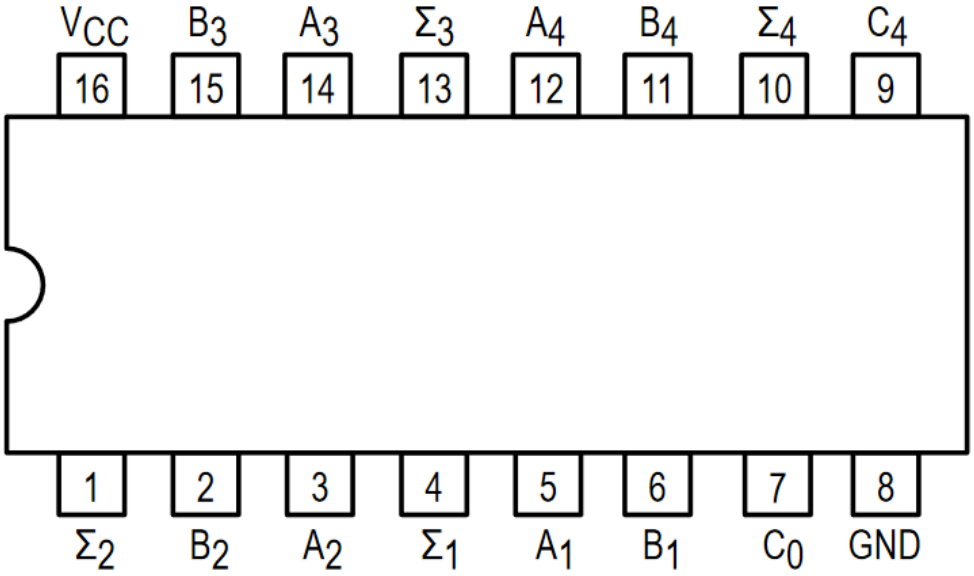
BITS Pilani
Hyderabad Campus
Department of Electrical Engineering

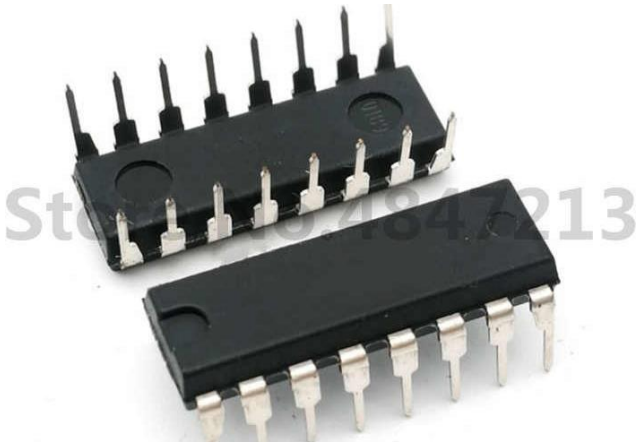
Digital Design : 2020-21
Lab 3
4-Bit Parallel Adder & BCD Adder

By Dr. Sanjay Vidhyadharan



4-Bit Adder

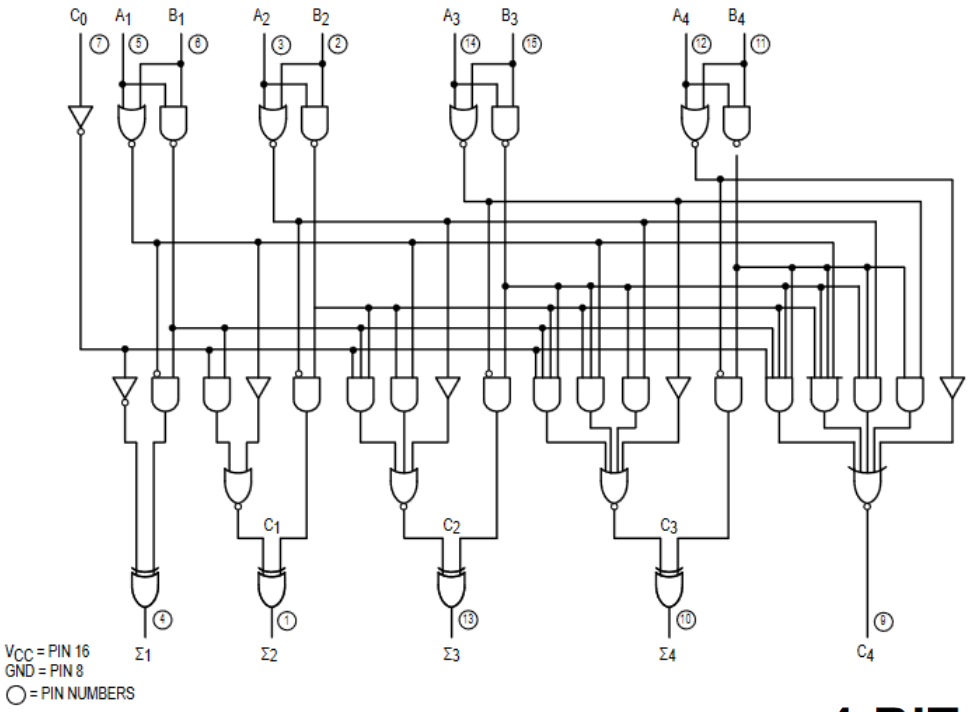




74283

4-Bit Adder

LOGIC DIAGRAM

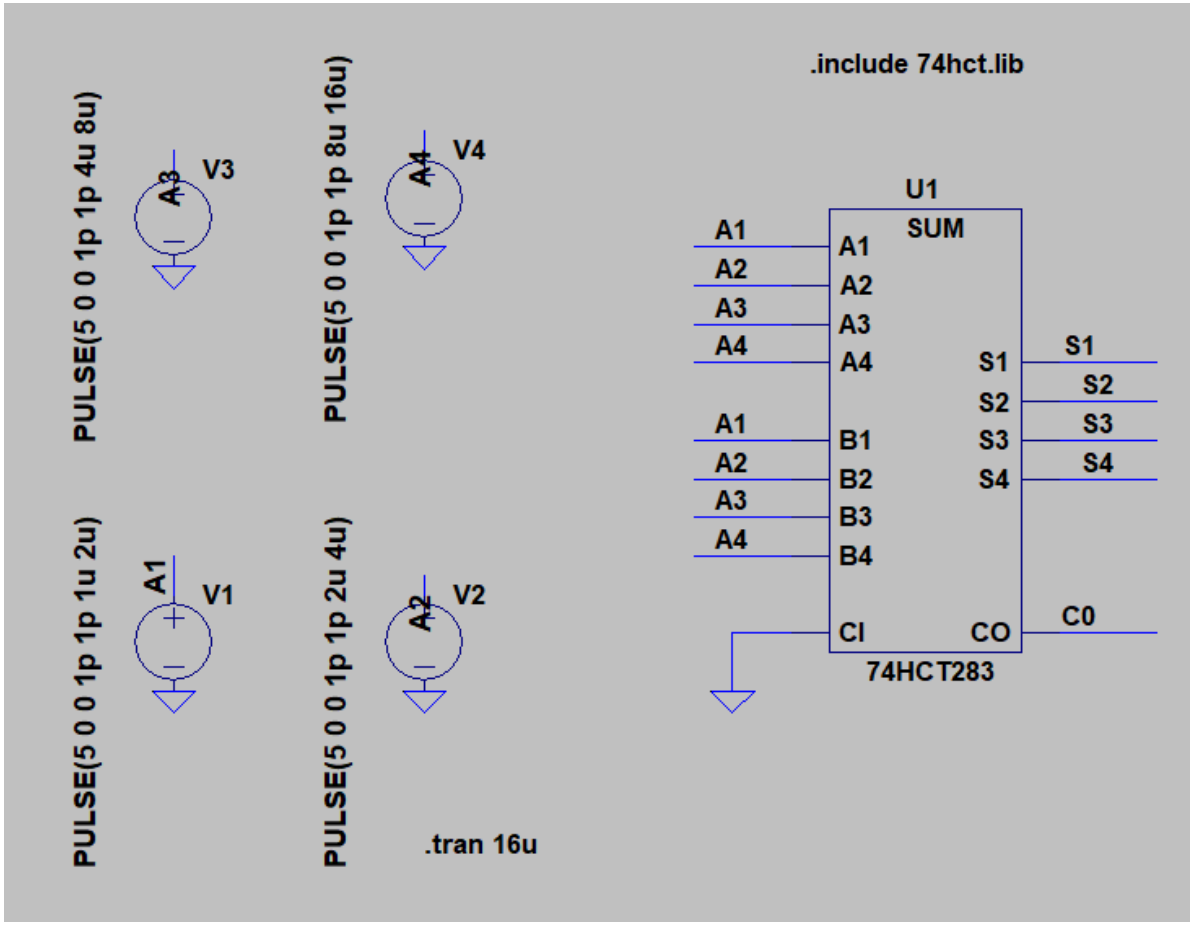


4-BIT BINARY FULL ADDER WITH FAST CARRY

The SN54/74LS283 is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words ($A_1 - A_4$, $B_1 - B_4$) and a Carry Input (C_0). It generates the binary Sum outputs ($\Sigma 1 - \Sigma 4$) and the Carry Output (C_4) from the most significant bit. The LS283 operates with either active HIGH or active LOW operands (positive or negative logic).

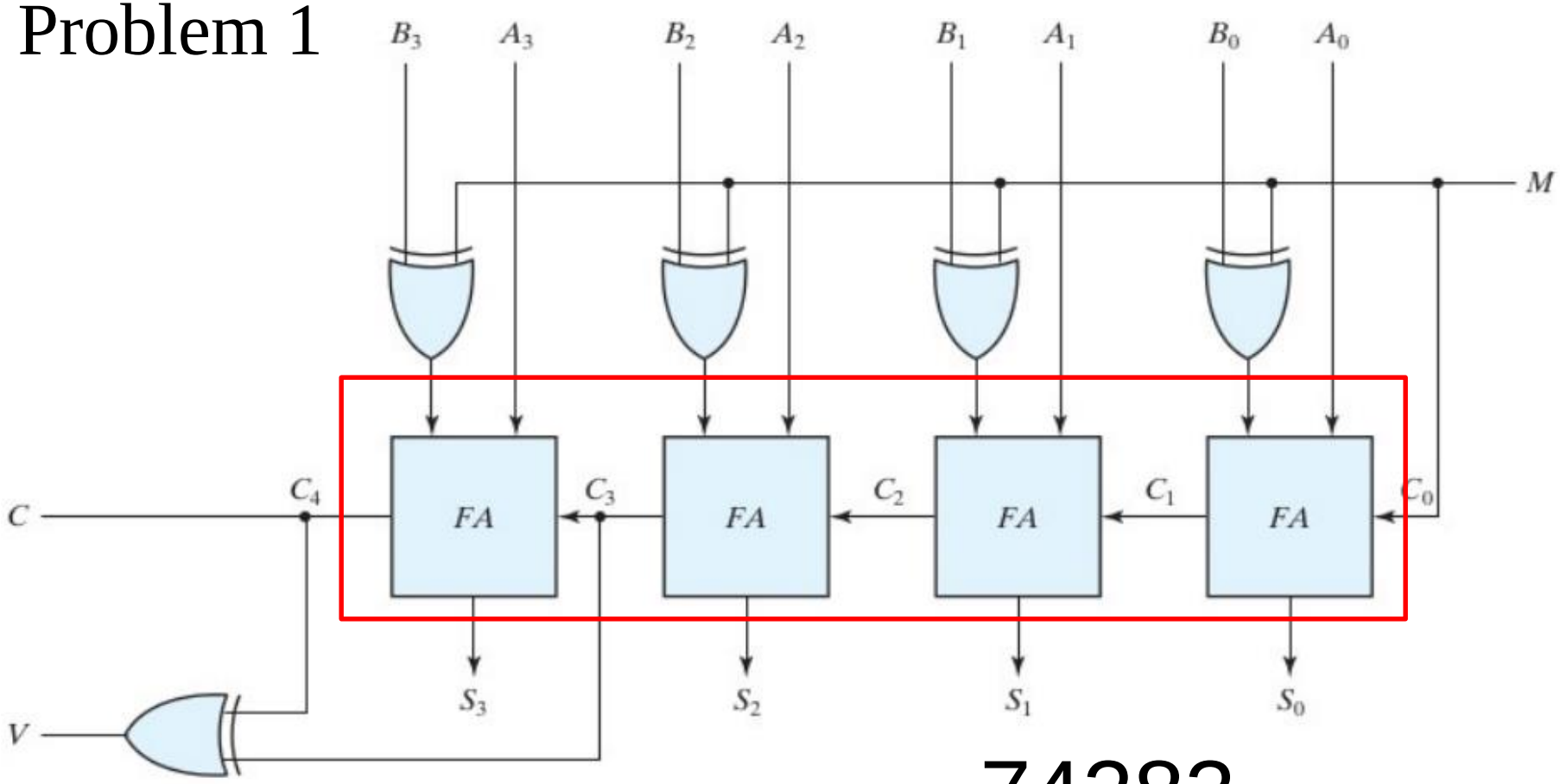
4-Bit Parallel Adder

Demo



4-Bit Adder Subtractor

Problem 1



74283

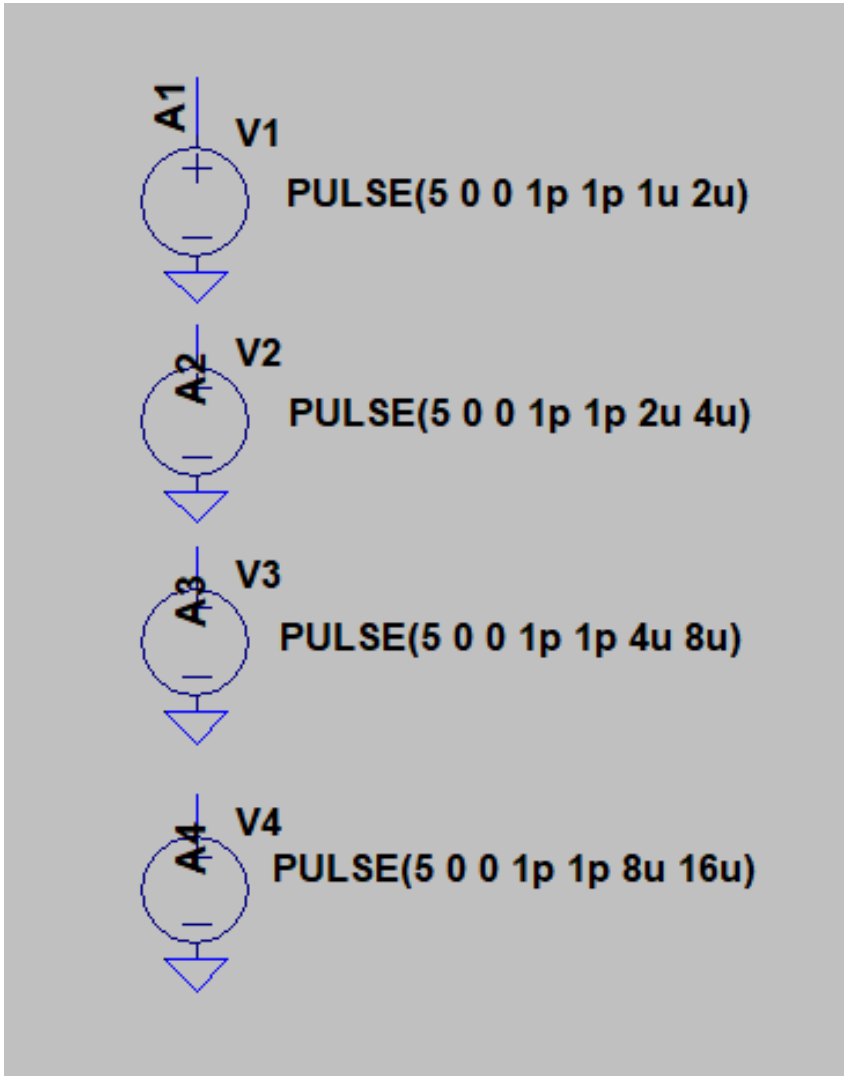
4-Bit Adder Subtractor

Problem 1

Signed 2's compl (n=4)	decimal value
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	$7=2^{n-1}-1$
1000	$-8=-2^{n-1}$
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

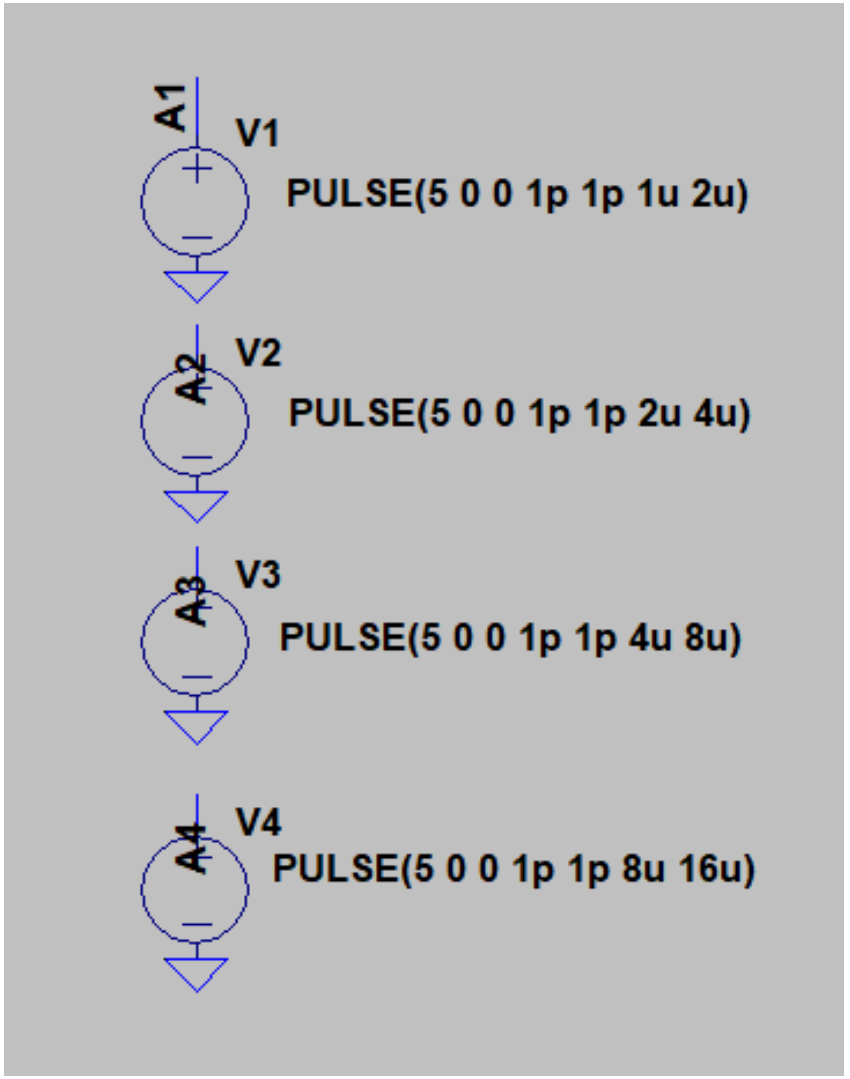
4-Bit Adder Subtractor

A	B	M	Sum	Remarks
0	4	0		
1	4	0		
2	4	0		
3	4	0		
4	4	0		Overflow
5	4	0		Overflow
6	4	0		Overflow
7	4	0		Overflow
-8	4	0		
-7	4	0		
-6	4	0		
-5	4	0		
-4	4	0		
-3	4	0		
-2	4	0		
-1	4	0		



4-Bit Adder Subtractor

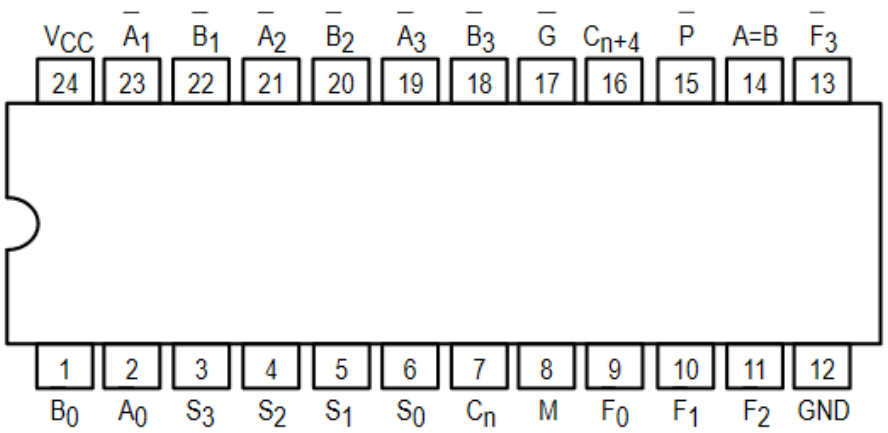
A	B	M	Sum	Remarks
0	4	1		
1	4	1		
2	4	1		
3	4	1		
4	4	1		
5	4	1		
6	4	1		
7	4	1		
-8	4	1		Overflow
-7	4	1		Overflow
-6	4	1		Overflow
-5	4	1		Overflow
-4	4	1		
-3	4	1		
-2	4	1		
-1	4	1		



4-Bit Adder Subtractor

SN54/74LS181

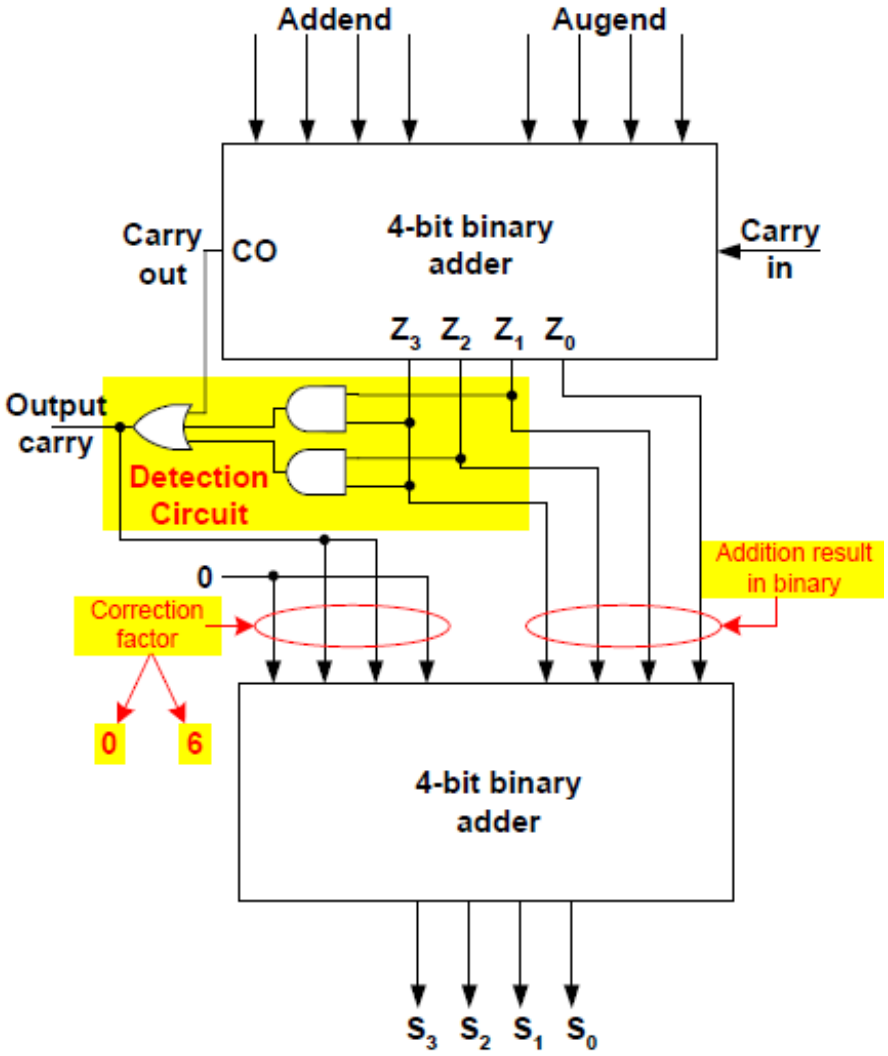
CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version
has the same pinouts
(Connection Diagram) as
the Dual In-Line Package.

BCD Adder

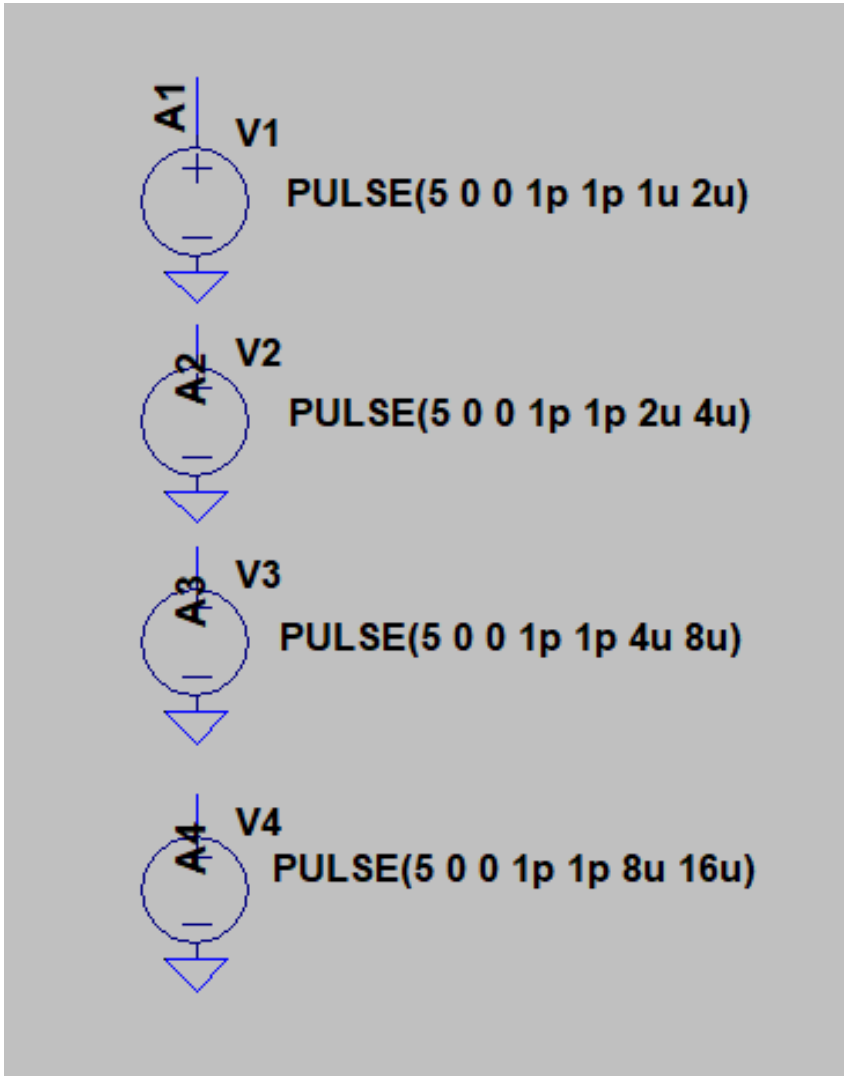
Problem 2



BCD Adder

A	B	Carry	Sum
0	0		
1	1		
2	2		
3	3		
4	4		
5	5		
6	6		
7	7		
8	8		
9	9		

Trans : 9u



Demonstration