BITS Pilani
Hyderabad Campus
Department of Electrical Engineering

Digital Design : 2020-21
Lab 2
Parity Generator & Adders

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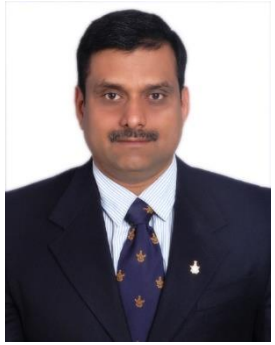


Parity Generator

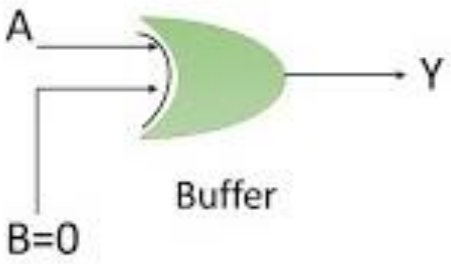
3-bit Message			Odd Parity Bit
X	Y	Z	
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

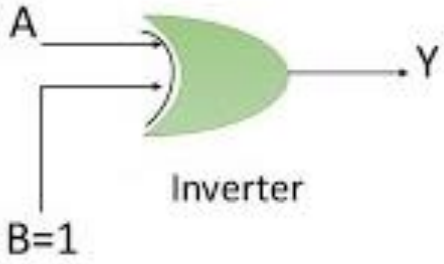
Parity Generator

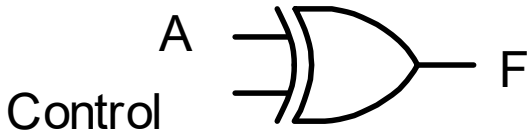
3-bit Message			Even Parity Bit
X	Y	Z	
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Parity Generator

EX-OR Gate As Buffer and Inverter

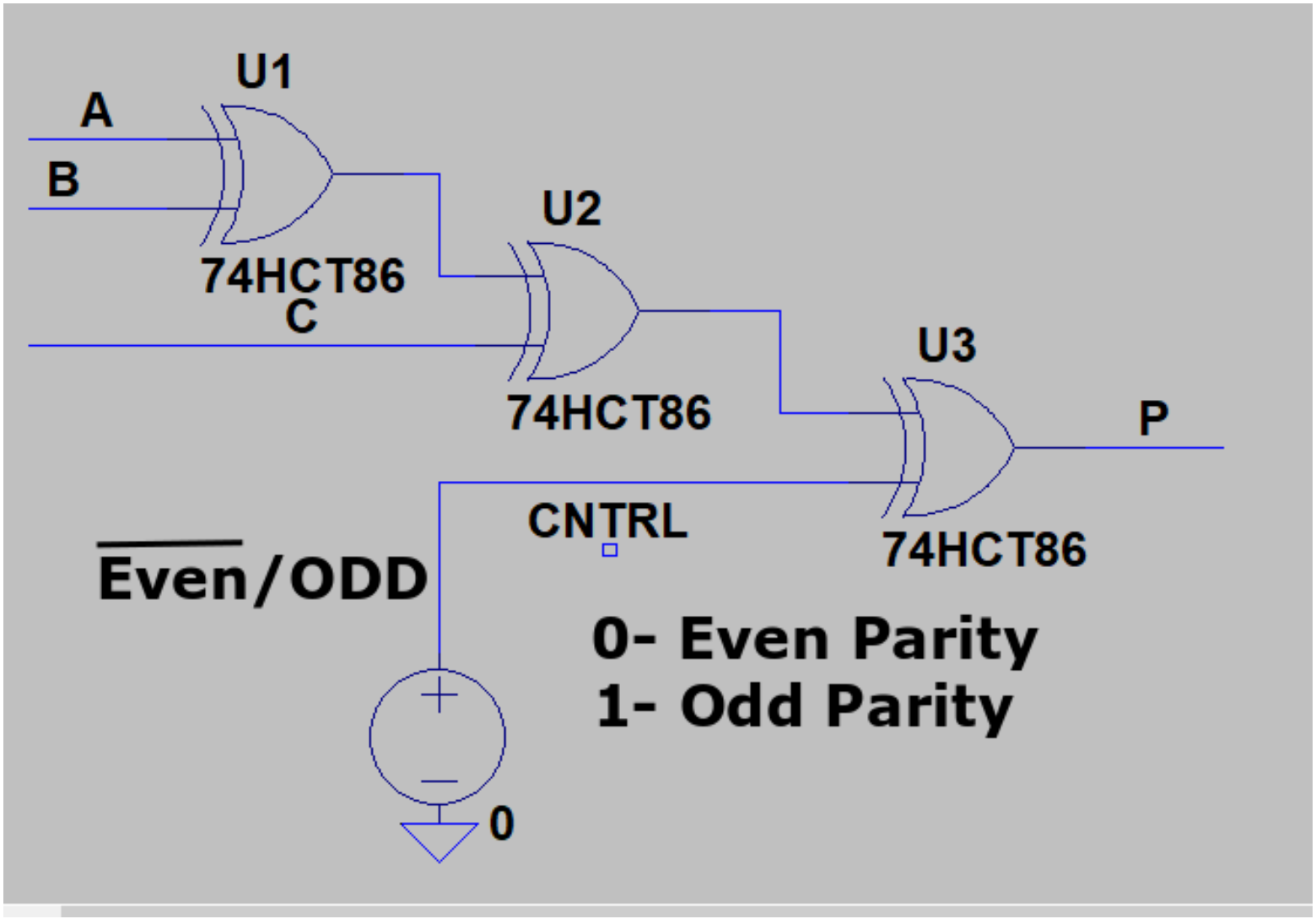






Control	A	F	
0	0	0	Pass
0	1	1	
1	0	1	Invert
1	1	0	

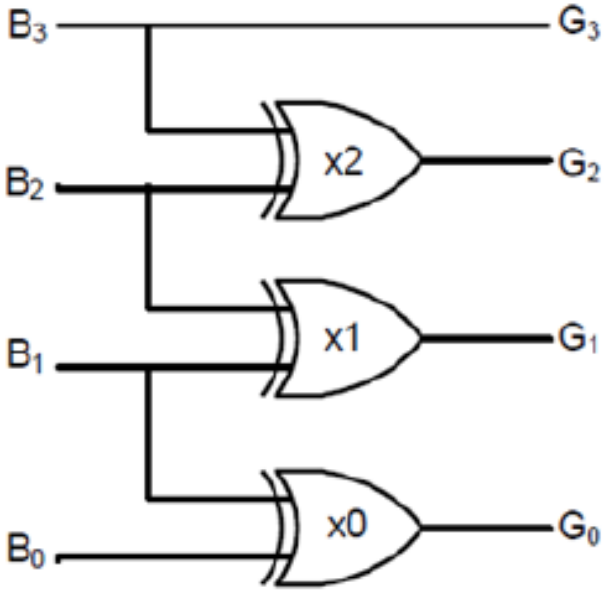
Parity Generator



Binary to Gray Converter

Problem 1:Binary to Gray Converter

Decimal Number	4 bit Binary Number ABCD	4 bit Gray Code $G_1G_2G_3G_4$
0	0 0 0 0	0 0 0 0
1	0 0 0 1	0 0 0 1
2	0 0 1 0	0 0 1 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 1 1 0
5	0 1 0 1	0 1 1 1
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 0 0
8	1 0 0 0	1 1 0 0
9	1 0 0 1	1 1 0 1
10	1 0 1 0	1 1 1 1
11	1 0 1 1	1 1 1 0
12	1 1 0 0	1 0 1 0
13	1 1 0 1	1 0 1 1
14	1 1 1 0	1 0 0 1
15	1 1 1 1	1 0 0 0



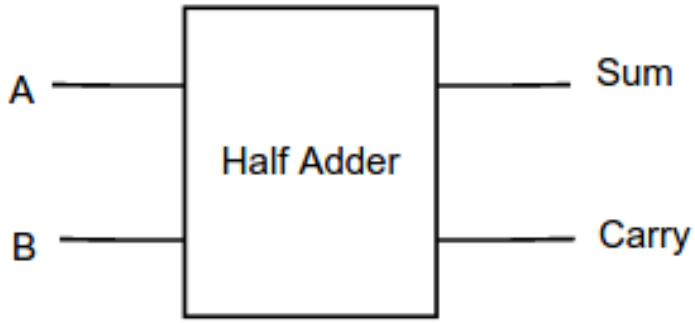
Half Adder

Problem 2: Half Adder

Truth Table

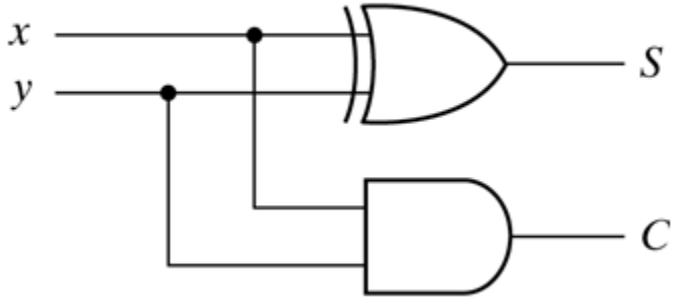
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Block Diagram



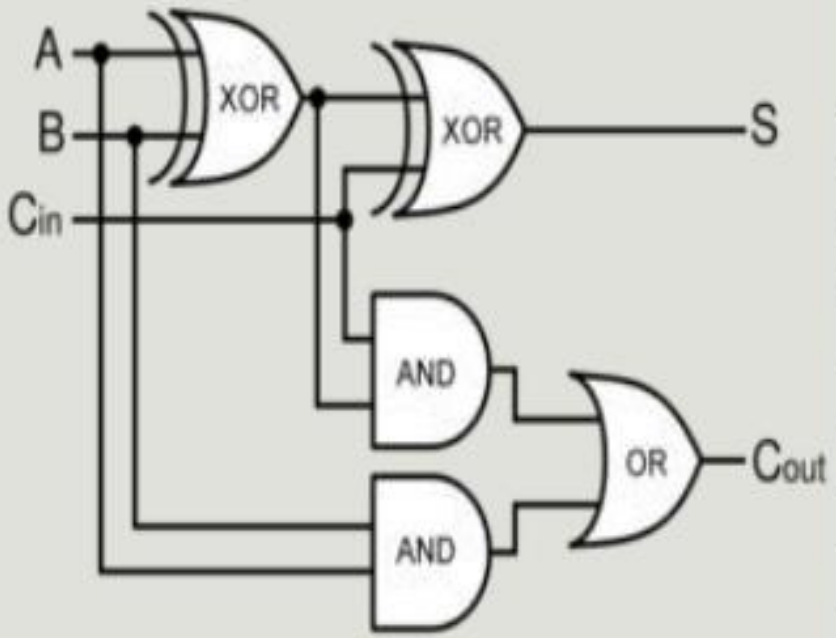
$$Sum(S) = x \oplus y$$

$$Carry(C) = xy$$



Full Adder

Problem 3: Full Adder



INPUT		CARRY IN	OUTPUT	
x	y	C_{in}	C_{out}	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

FULL ADDER CIRCUIT & TRUTH TABLE

Demonstration