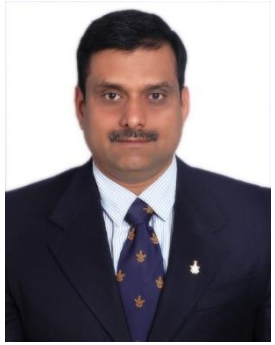
BITS Pilani
Hyderabad Campus
Department of Electrical Engineering

Digital Design : 2020-21
Lab 1

By Dr. Sanjay Vidhyadharan



BITS Pilani
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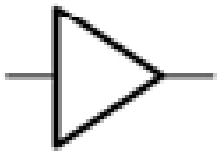
Outline

- Review of Digital Gates
- Digital Logic families
- Few 74XX series TTL Digital ICs
- Procedure for installation of LT SPICE
- Problem definition for DD: Lab 1
- Demonstration of LT SPICE installation and simulation.

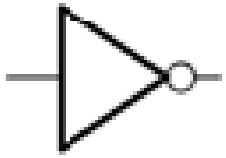
Review of Digital Gates

YES



INPUT	OUTPUT
A	
0	0
1	1

NOT



INPUT	OUTPUT
A	
0	1
1	0

Review of Digital Gates

AND

INPUT		OUTPUT
A	B	
0	0	0
1	0	0
0	1	0
1	1	1

OR

INPUT		OUTPUT
A	B	
0	0	0
1	0	1
0	1	1
1	1	1

XOR

INPUT		OUTPUT
A	B	
0	0	0
1	0	1
0	1	1
1	1	0

Review of Digital Gates

NAND

INPUT		OUTPUT
A	B	
0	0	1
1	0	1
0	1	1
1	1	0

NOR

INPUT		OUTPUT
A	B	
0	0	1
1	0	0
0	1	0
1	1	0

XNOR

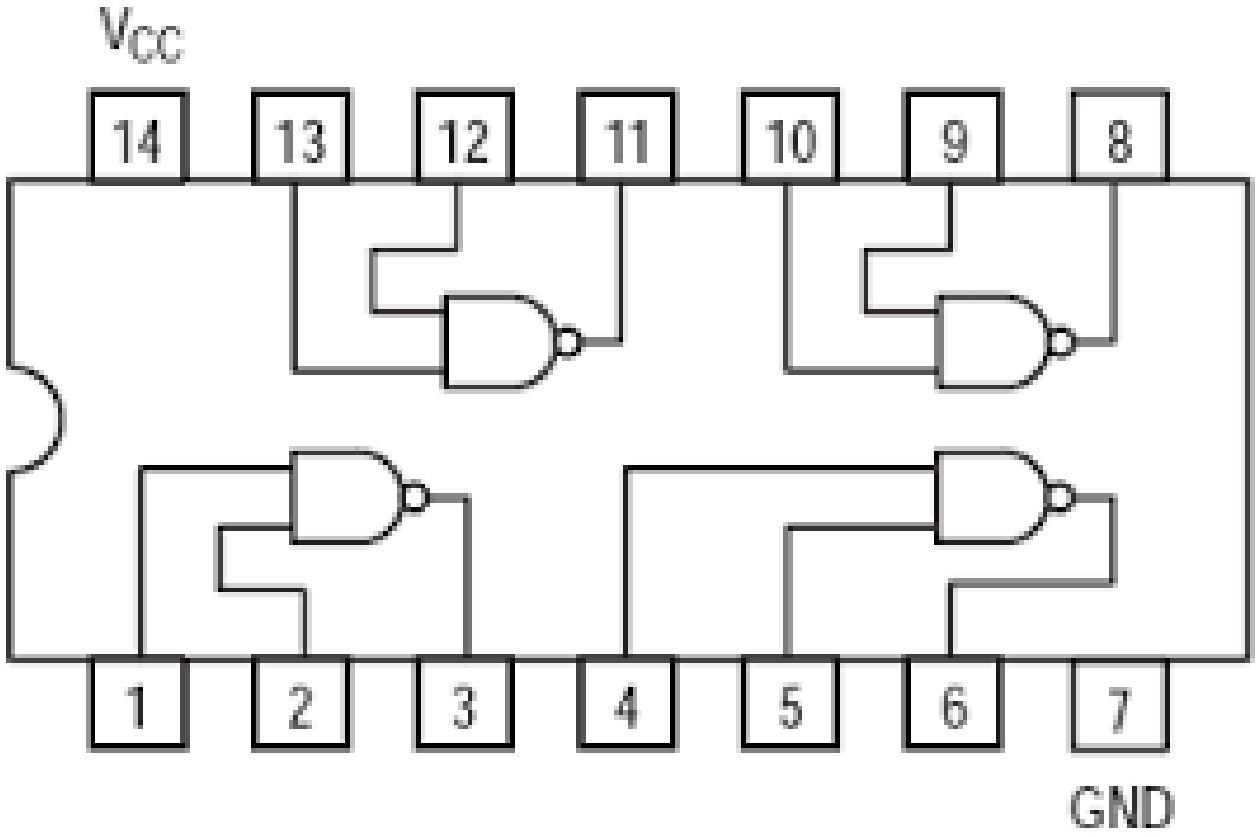
INPUT		OUTPUT
A	B	
0	0	1
1	0	0
0	1	0
1	1	1

Digital Logic families

- Diode Transistor Logic : 1959
- Resistor Transistor Logic : 1961
- Transistor Transistor Logic : 1963 Discrete IC
- Emitter-coupled logic : First Microprocessor 360
- CMOS :
  - 1974 Intel 4004 which had 2000 Transistors
    Channel Length of 10 µm.
  - 2020 AMB 7 nm has billions of Transistors
    Channel Length of 7 nm.

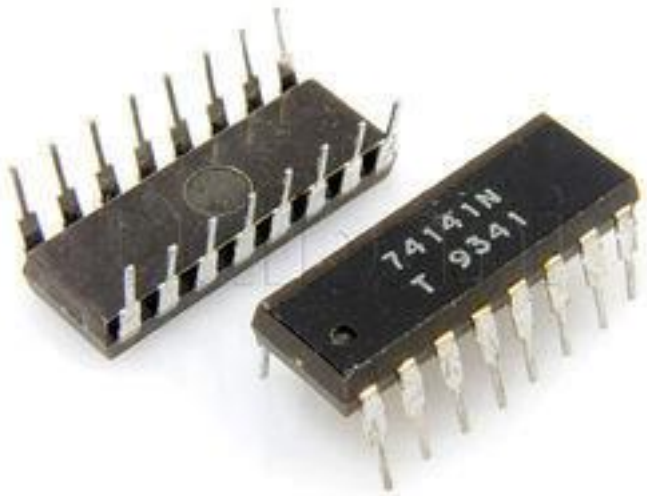
74XX Series TTL ICs

7400 Quad 2 Input NAND

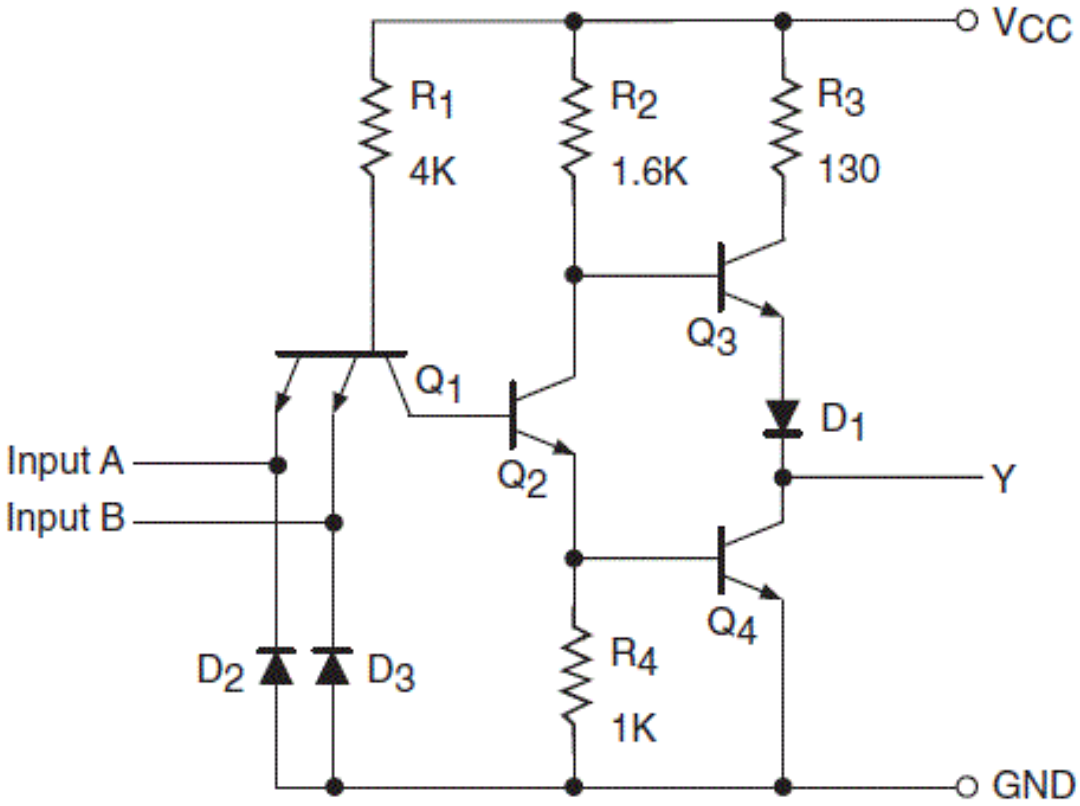


74XX Series TTL ICs

7400 NAND



TTL Gate



TTL 2 input NAND Gate

74XX Series TTL ICs

7400 NAND DATA SHEET

FAIRCHILD
SEMICONDUCTOR™

September 1986
Revised July 2001

DM7400
Quad 2-Input NAND Gates

General Description

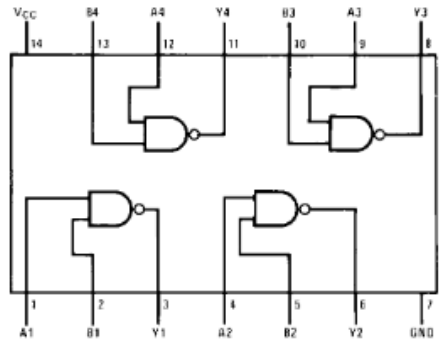
This device contains four independent gates each of which performs the logic NAND function.

Ordering Code:

Order Number	Package Number	Package Description
DM7400M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
DM7400N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

DM7400 Quad 2-Input NAND Gates

74XX Series TTL ICs

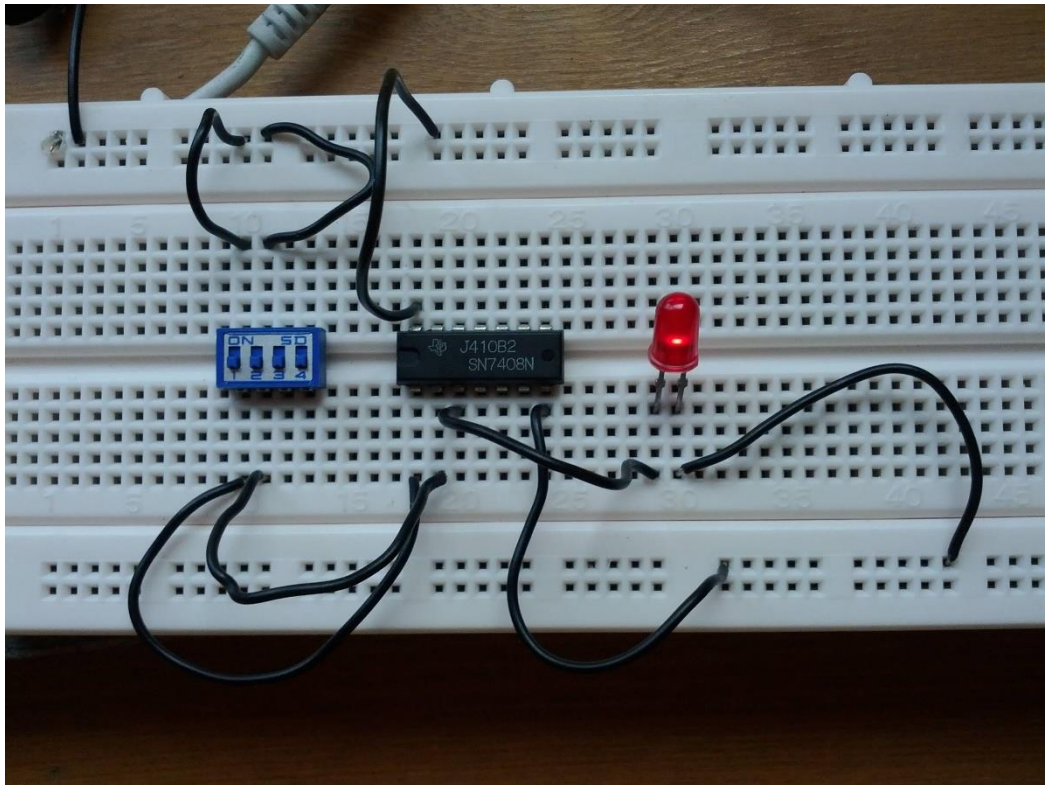
7400 NAND DATA SHEET

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C

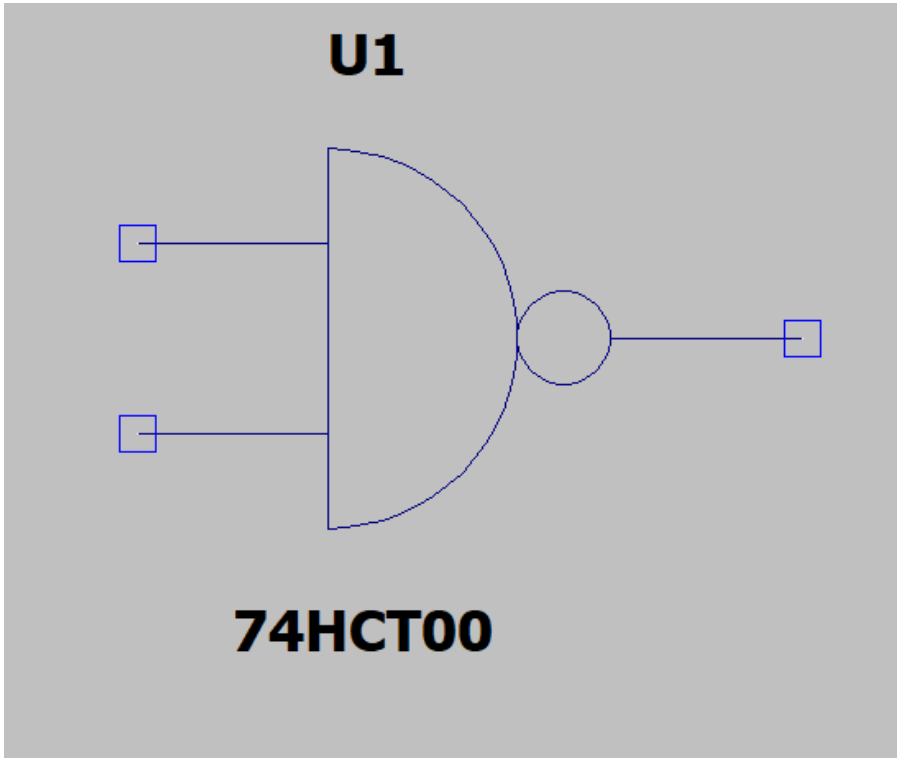
74XX Series TTL ICs

7400 NAND



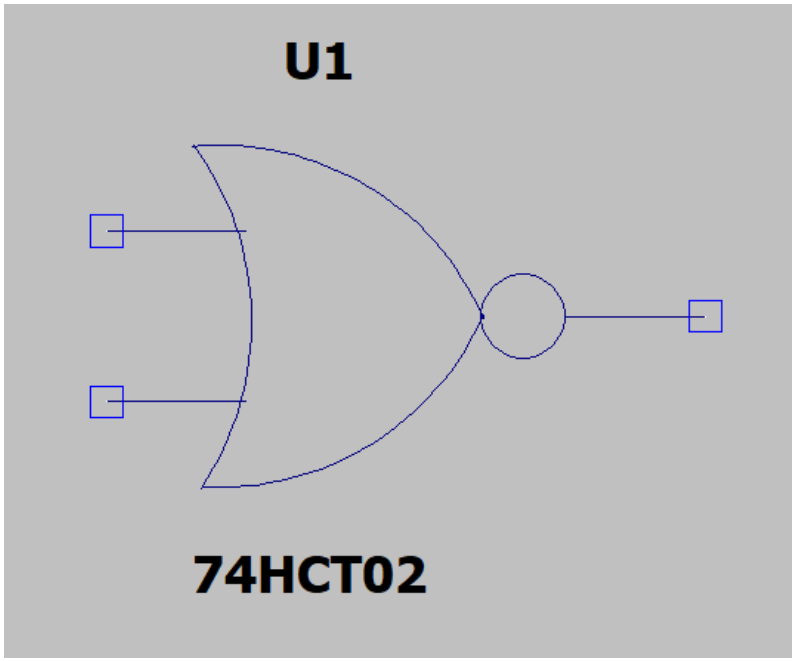
74XX Series TTL ICs

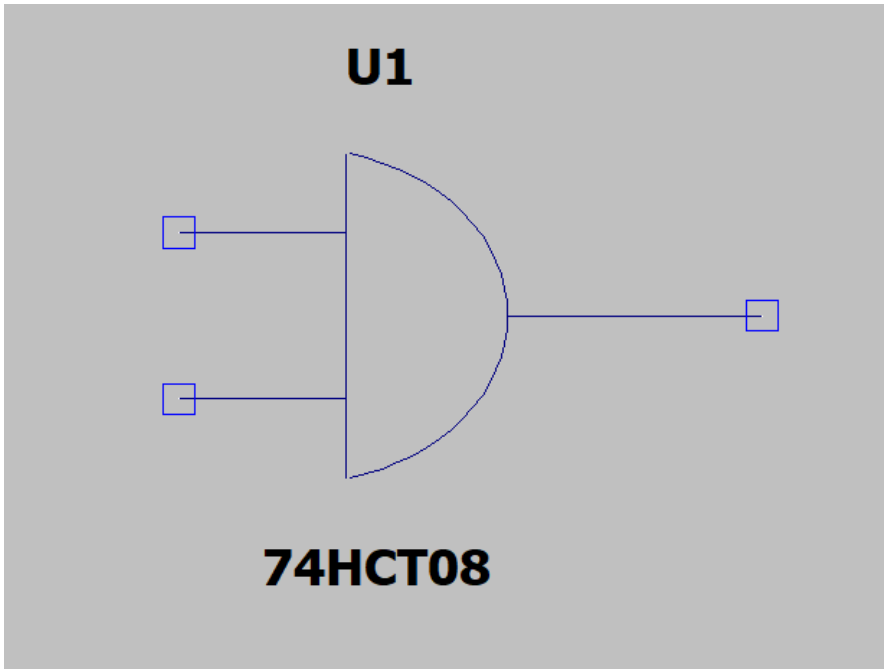
7400 NAND MODEL IN LT SPICE



74XX Series TTL ICs

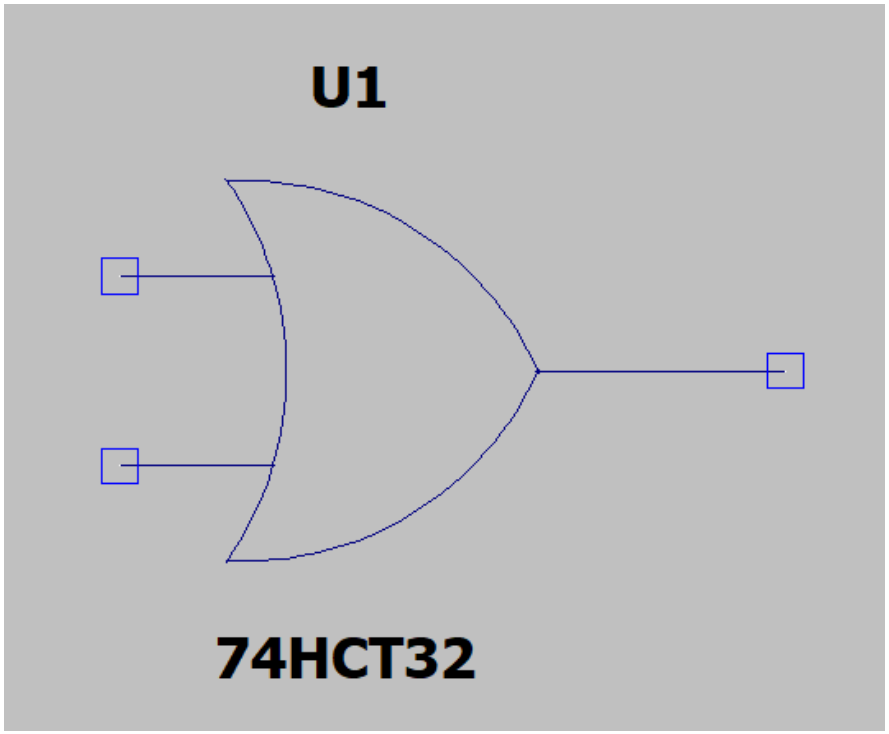
MODELS IN LT SPICE

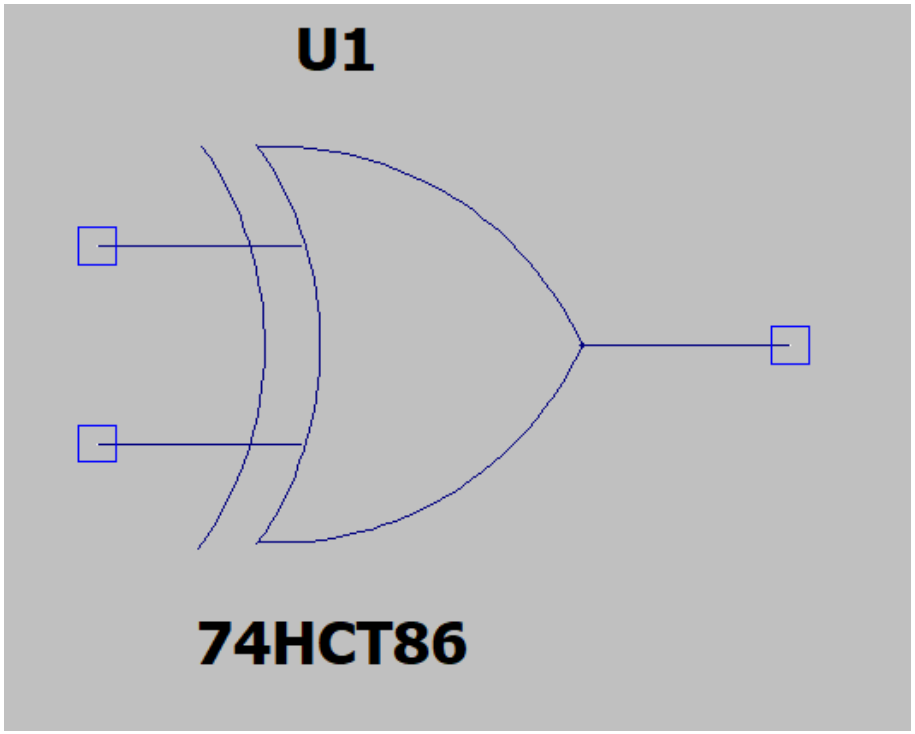




74XX Series TTL ICs

MODELS IN LT SPICE





Procedure for Installation of LT SPICE

Installing 74XX SPICE Model in LT SPICE

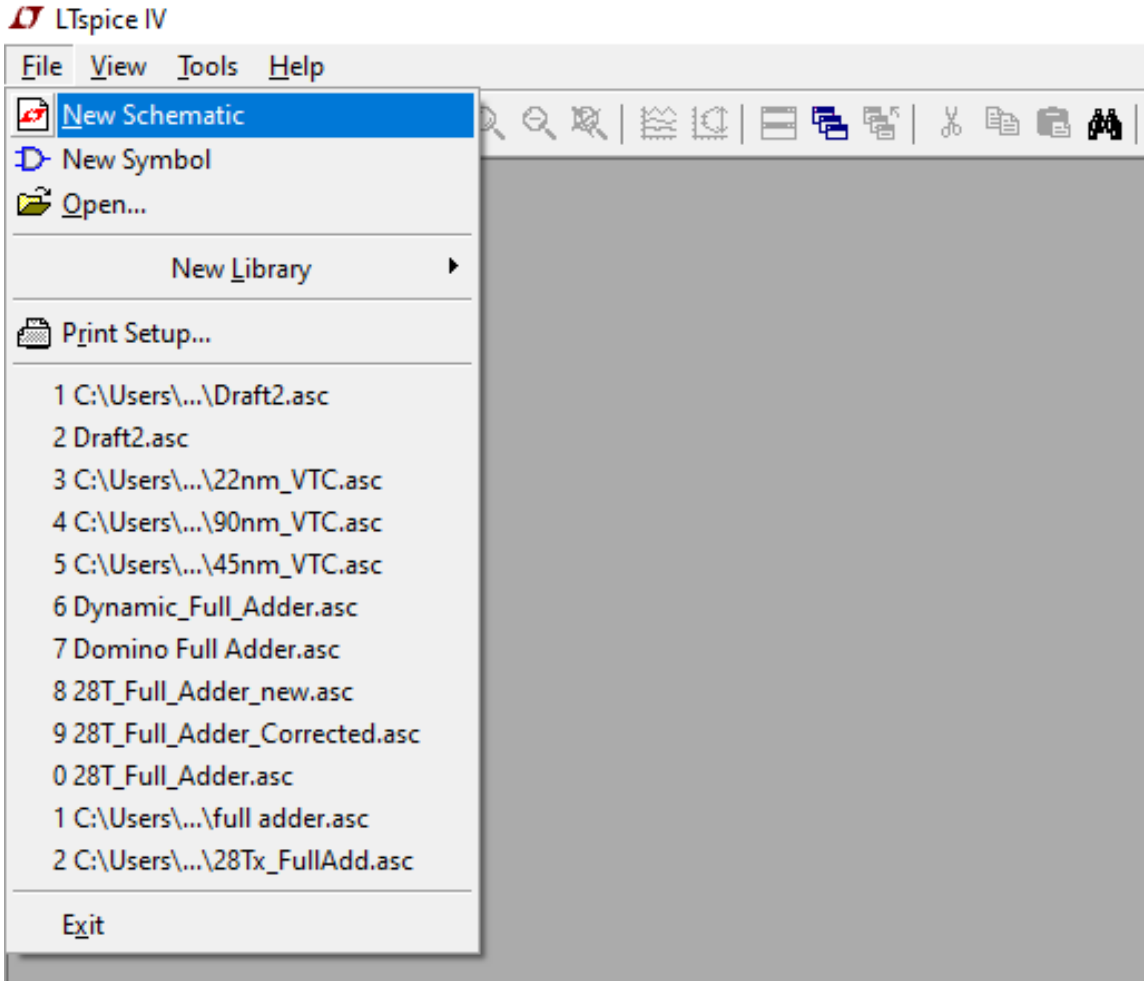
1. Download file “LT_SPICE_Installation_Files.zip” from https://sanjayvidhyadharan.in/Downloads

2. Unzip the file. It contains the following files/folder
   (a) ltspiceiv.exe
   (b) 74hct.lib
   (c) Sym (Folder)
   (d) Example1.asc

3. Run the ltspiceiv.exe file to install LTSPICE on to your PC/laptop.

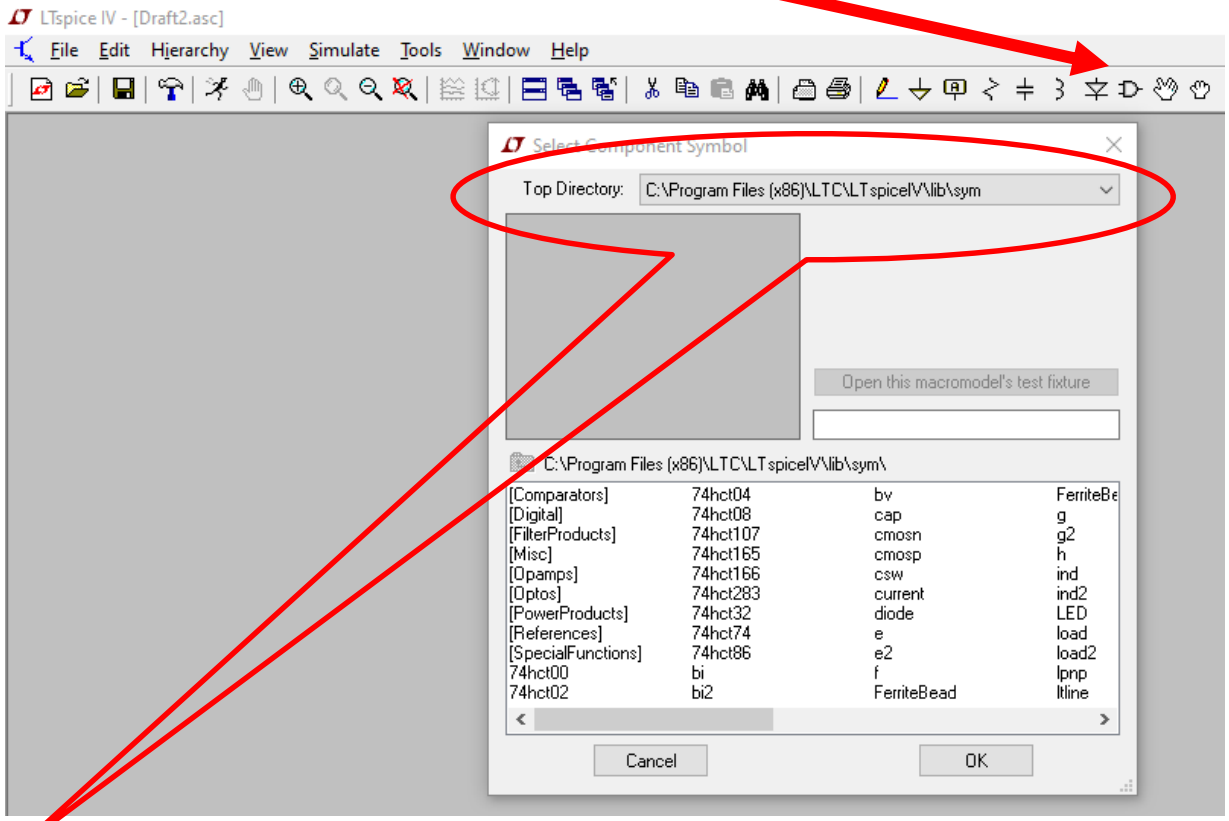
Procedure for Installation of LT SPICE

4. Open LtSpice. And open a New Schematic from File tab.



Procedure for Installation of LT SPICE

5. Click on the Component tab (looks like a AND gate) on the new schematic window



6. Note the path of the LT SPICE lib file

Procedure for Installation of LT SPICE

7. Copy paste 74ct.lib file in the folder

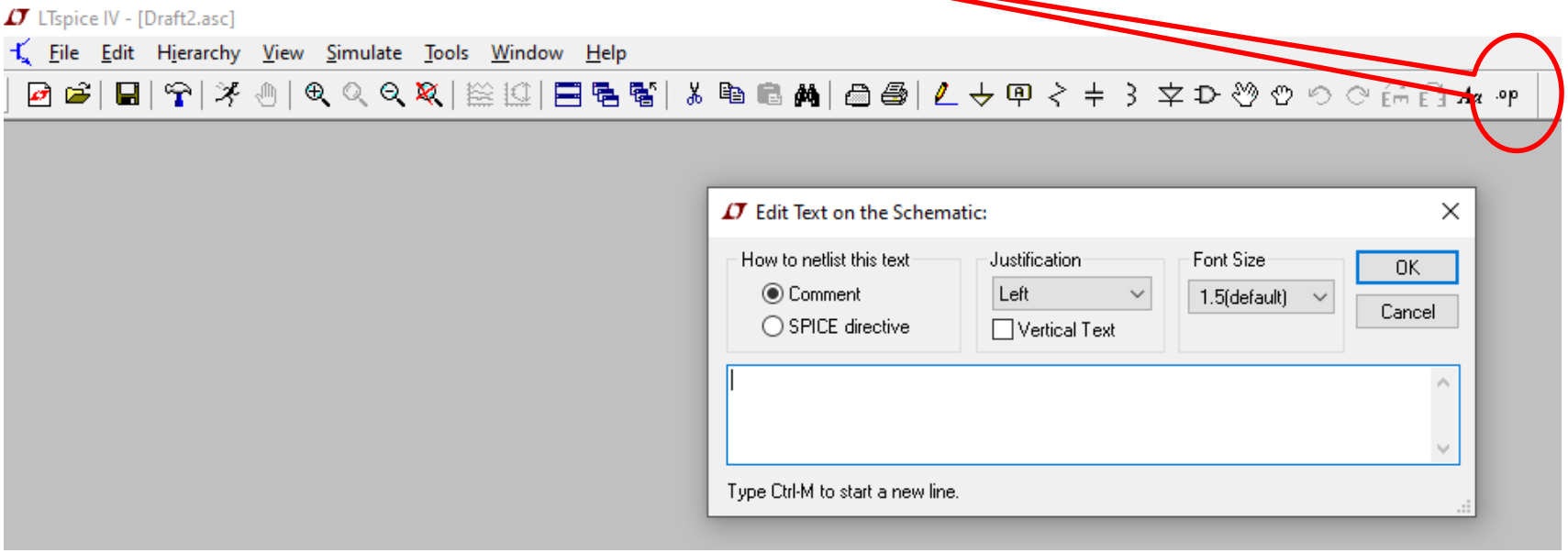
C:\Program Files\LTC\LTspiceIV\lib\sub

8. Copy paste all the files contained in downloaded folder "Sym" into

C:\Program Files\LTC\LTspiceIV\lib\sym

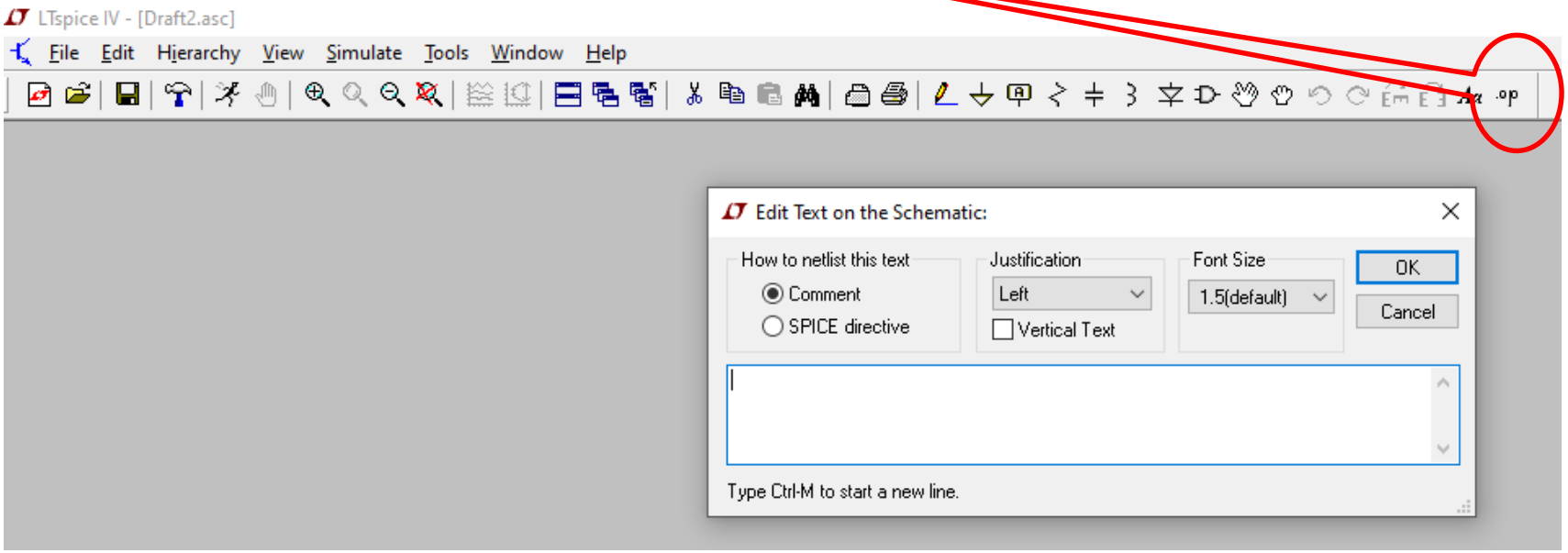
Procedure for Installation of LT SPICE

9. Click on the SPICE Directive tab as shown below:-



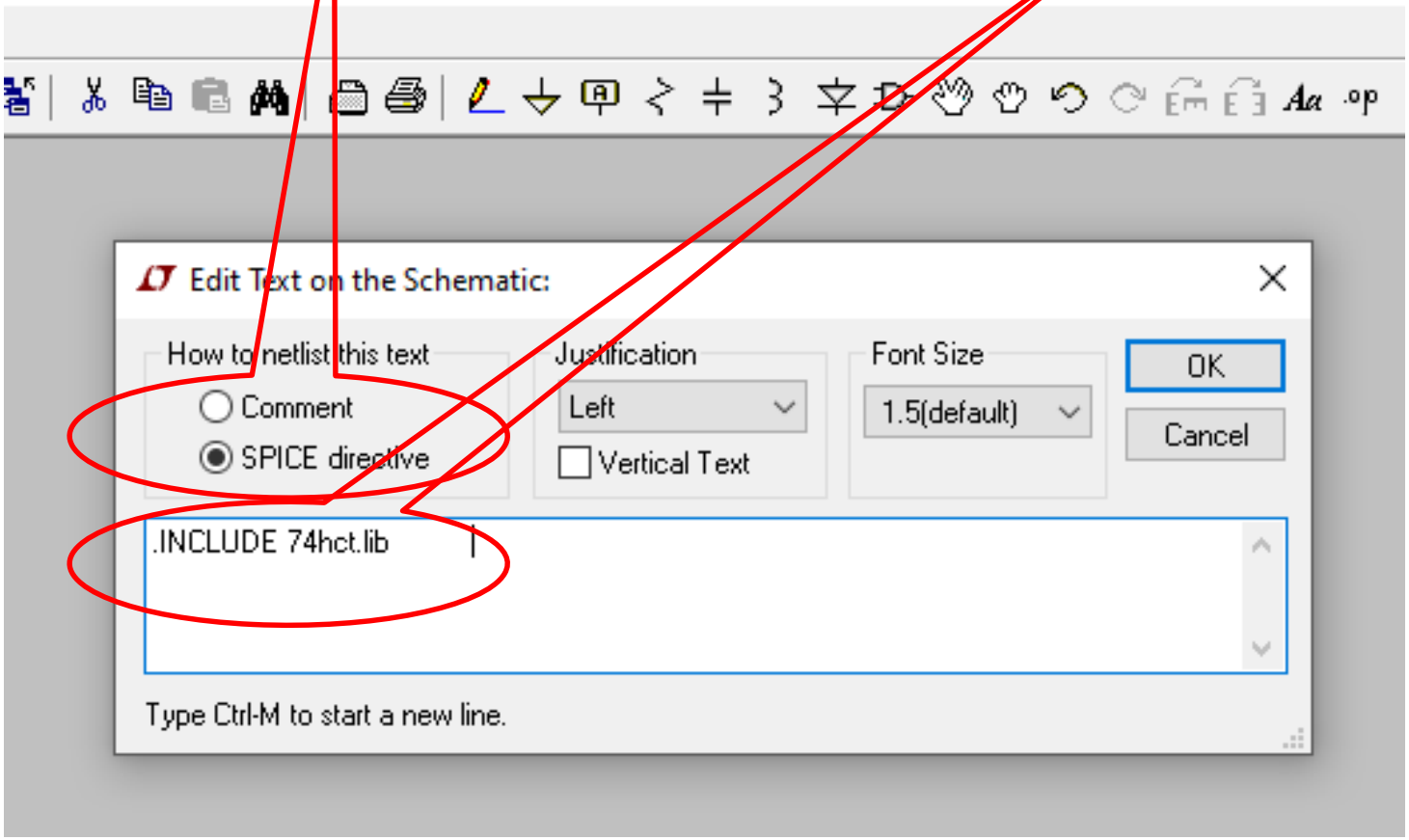
Procedure for Installation of LT SPICE

9. Click on the SPICE Directive tab as shown below:-



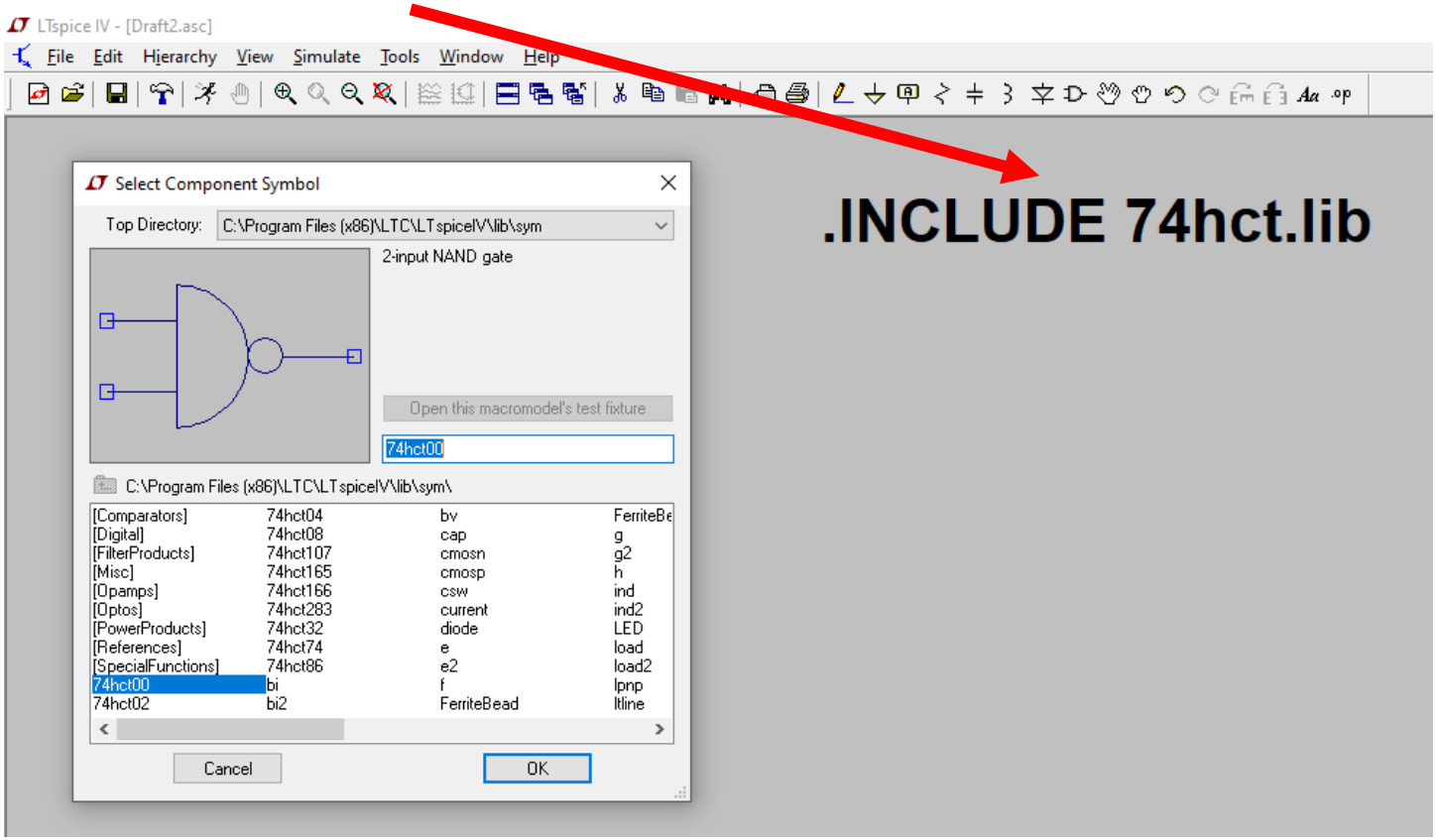
Procedure for Installation of LT SPICE

10. Select SPICE Directive and Type .INCLUDE 74hct.lib



Procedure for Installation of LT SPICE

10. Place the SPICE directive on the schematic

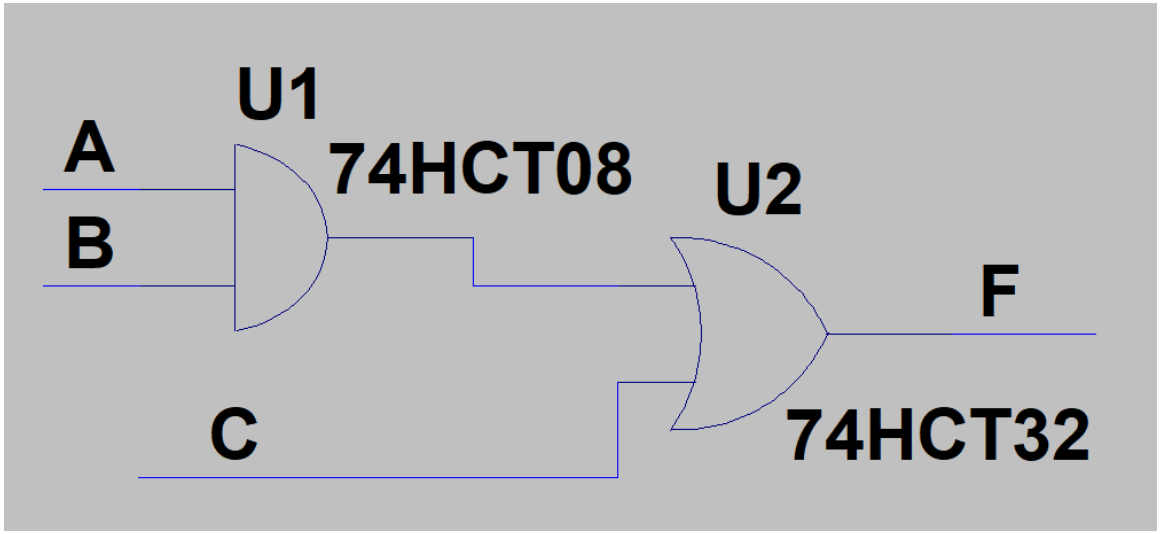


11. Select the component tab and you will be able to see the 74XX series gates.

Problem Definition for DD: Lab 1

Sample Run

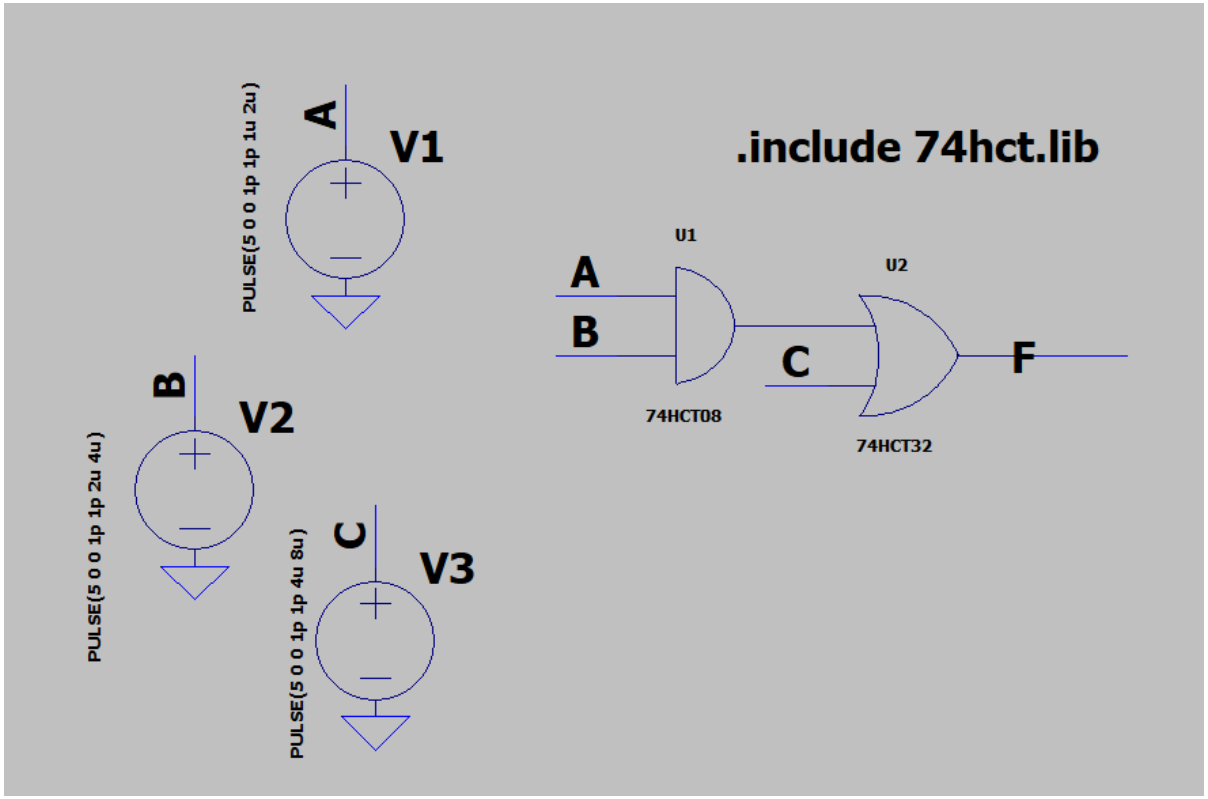
F= AB+C (Implementation with AND & OR Gates)



Problem Definition for DD: Lab 1

Sample Run

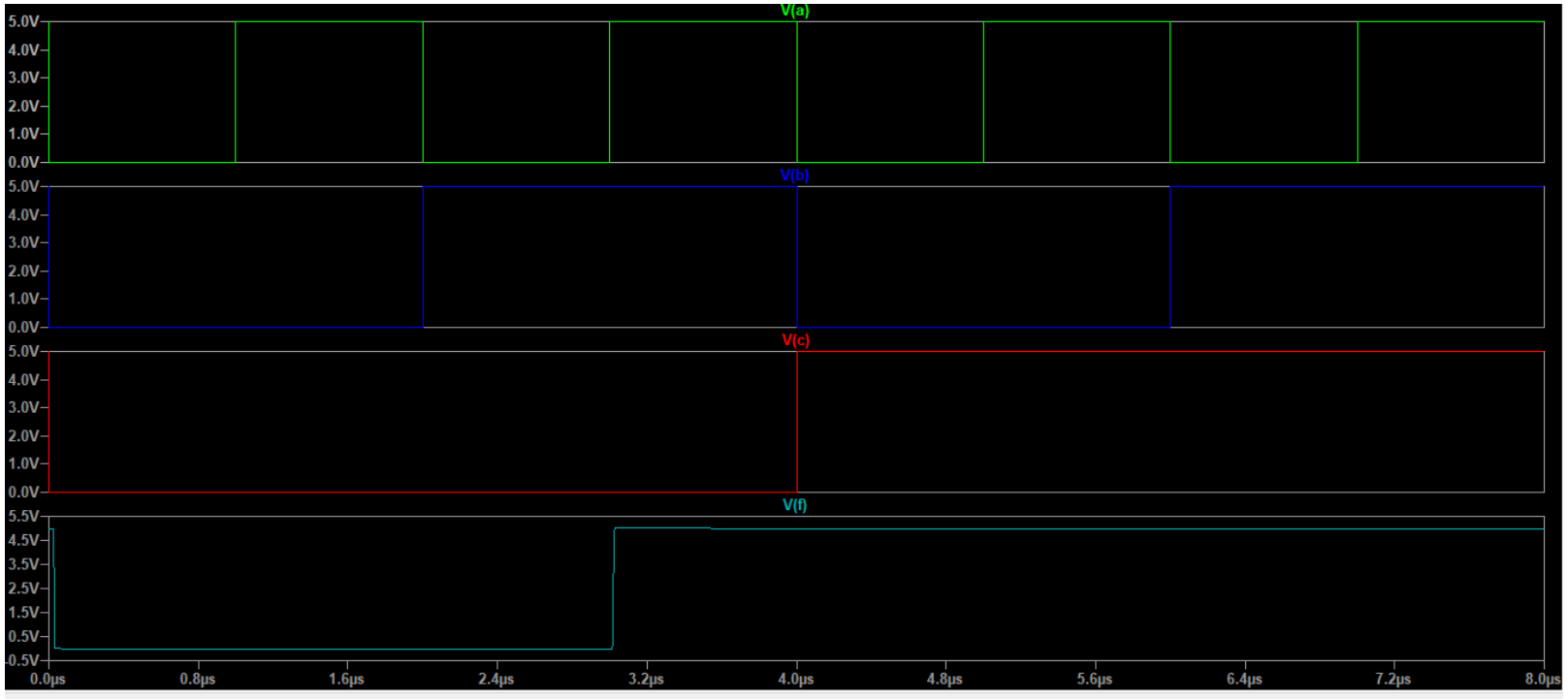
F= AB+C (Implementation with AND & OR Gates)



Problem Definition for DD: Lab 1

Sample Run

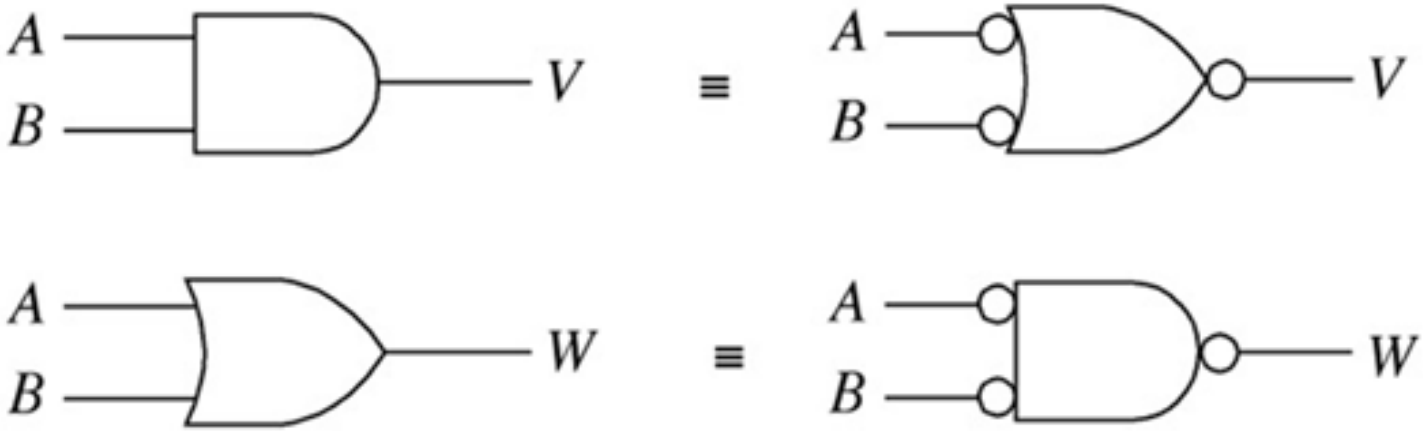
F= AB+C (Implementation with AND & OR Gates)



Problem Definition for DD: Lab 1

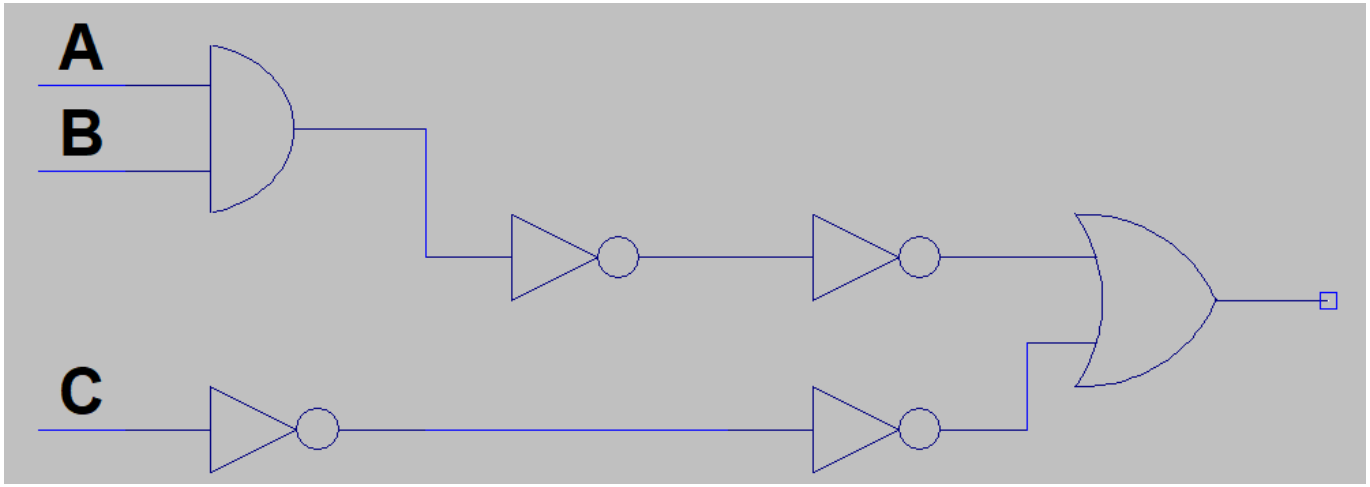
Sample Run

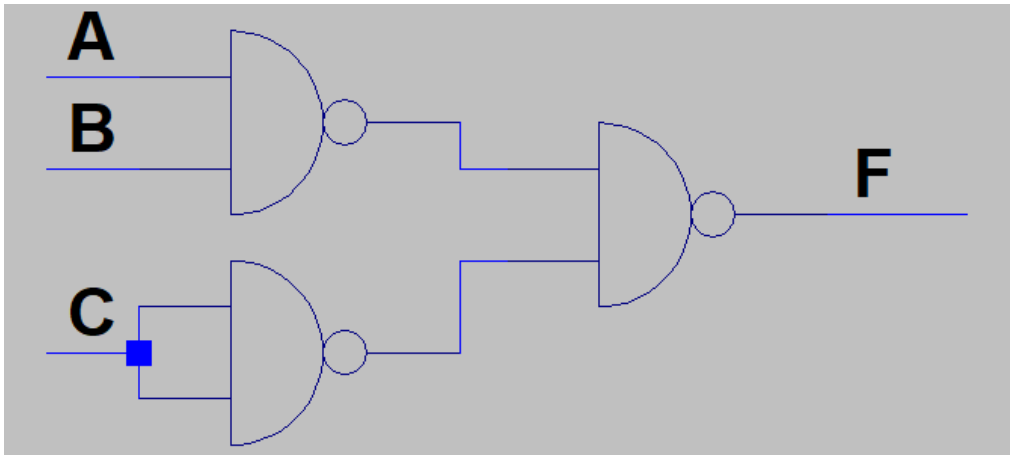
F= AB+C (Implementation with NAND Gates)



Problem Definition for DD: Lab 1

Sample Run **F= AB+C** **Implementation with NAND Gates**





Problem Definition for DD: Lab 1

Problem 1: Implement the Majority Circuit

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$$F = AB + BC + CA + ABC$$

$$F = AB + BC + CA$$

Problem definition for DD: Lab 1

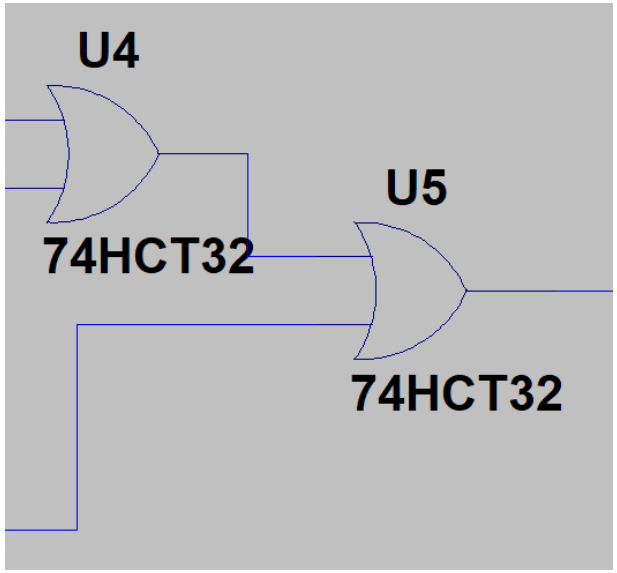
Problem 1: Implement the Majority Circuit

Run1 : Implement F with AND & OR gates

Check output for all combinations of Input

F= AB+BC+CA

Hint: Use Three 2 i/p AND & Two 2 i/p OR GATE



Problem definition for DD: Lab 1

Problem 1: Implement the Majority Circuit

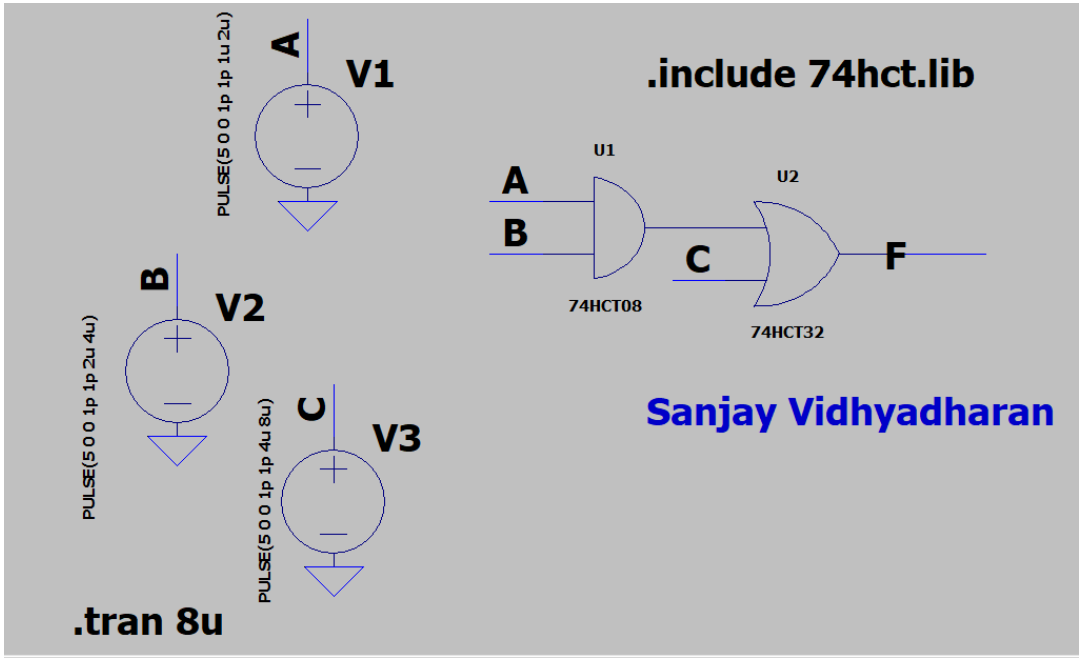
Run1 : Implement F with NAND gates

F= AB+BC+CA

Check output for all combinations of Input

Hint: Use Three 2 i/p NAND & One 3 i/p NAND GATE

Submission



Upload LTSPICE file to the folder given by your Lab instructor

1. With your name in the schematic as shown above

2. LT Spice File name indicating your Roll number

Eg. 2019H1240056H.asc

Demonstration