BITS Pilani
Hyderabad Campus
Department of Electrical Engineering

Digital Design : 2020-21
Lab 8
Sequential Circuit Design using D and JK Flipflops

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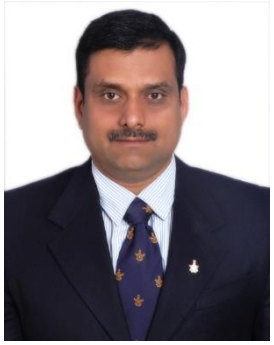
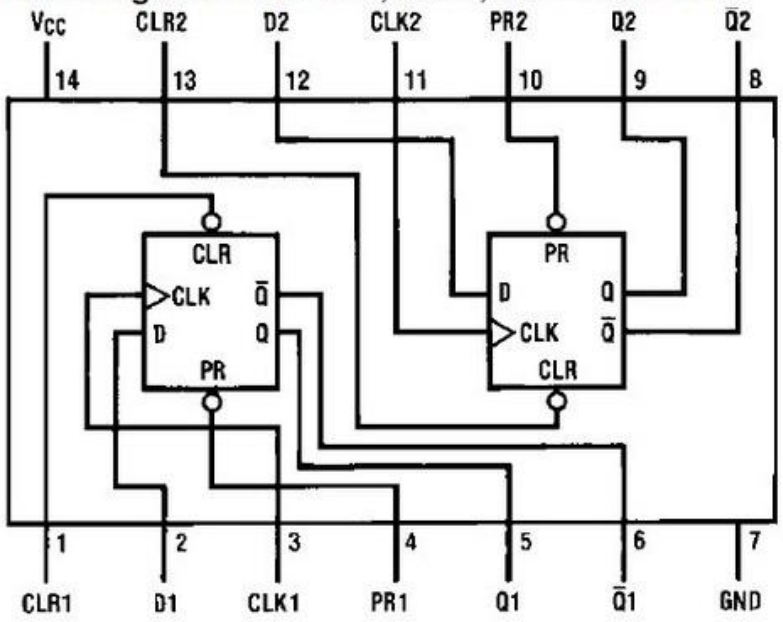


The 74HCT74 D Flipflop

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Truth Table

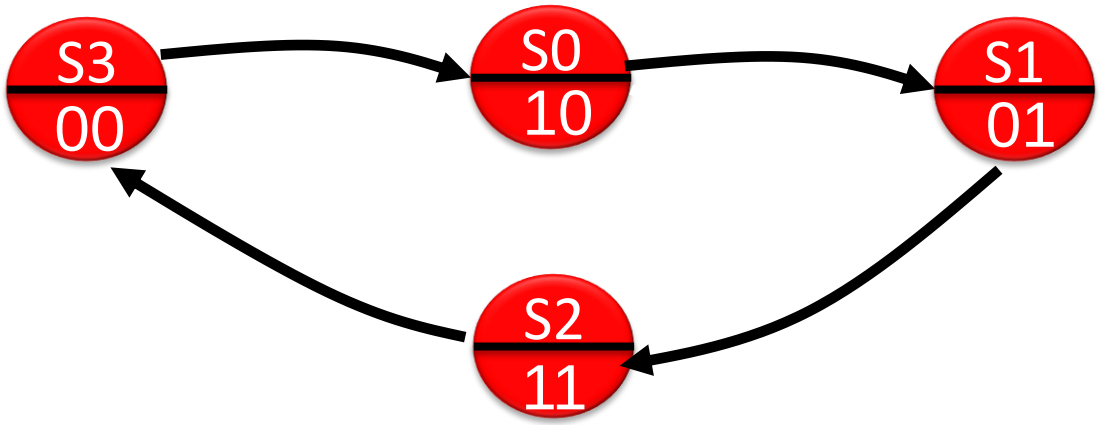
Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$ 0

Note: Q0 = the level of Q before the indicated input conditions were established.

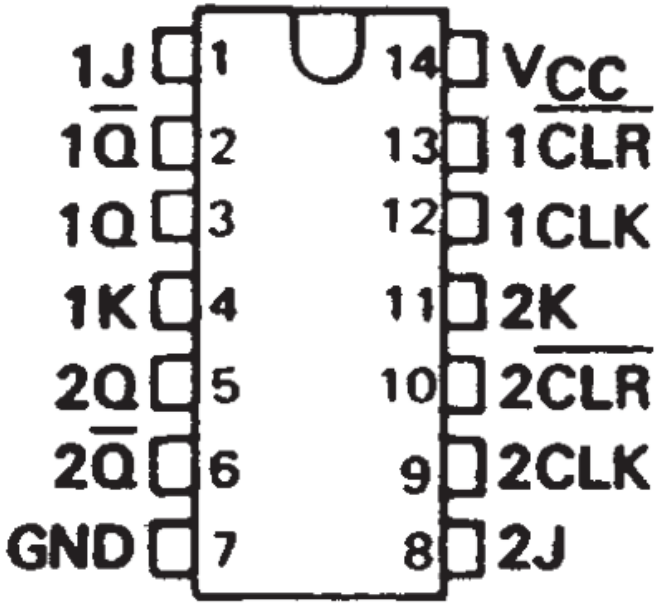
Note 1: This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (HIGH) level.

The 74HCT74 D Flipflop

Problem 1: Design a Counter using D-Flipflop as per state diagram given below:-



The 74HCT107 JK Flipflop



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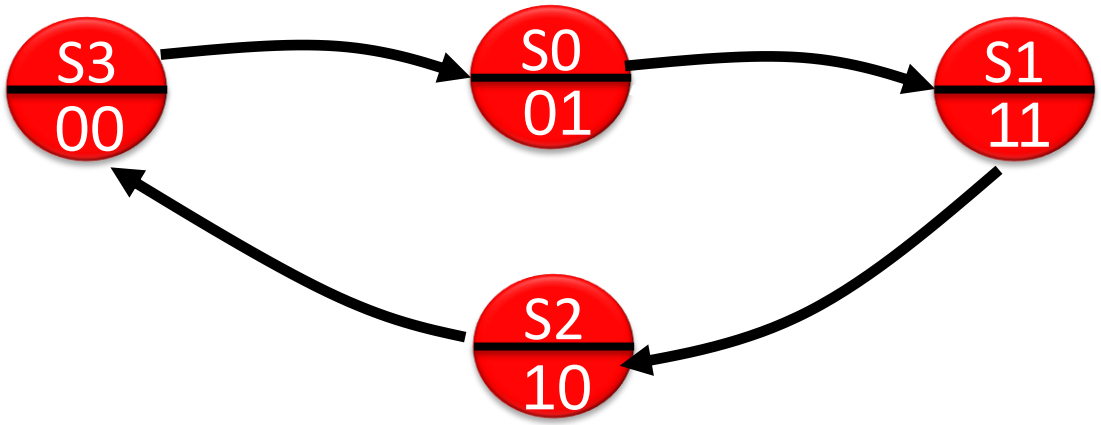
FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

The 74HCT74 D Flipflop

Problem 1: Design a Gray Counter using JK-Flipflop as per state diagram given below:-



Demonstration