BITS Pilani
Hyderabad Campus
Department of Electrical Engineering

Digital Design : 2020-21
Lab 6
Dataflow Modelling
Implementation of 4-Bit Adder & BCD Adder
in Xilinx ISE

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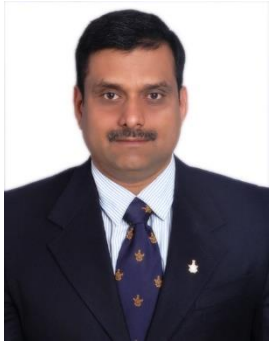

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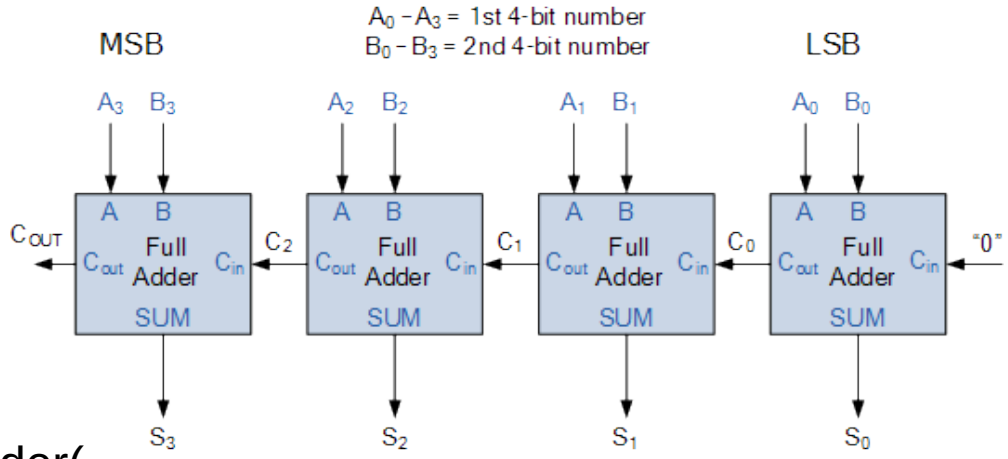
New Concepts

1. Handling multi-bit data

2. Concatenation to group data {}

Demonstration : 4-bit Adder



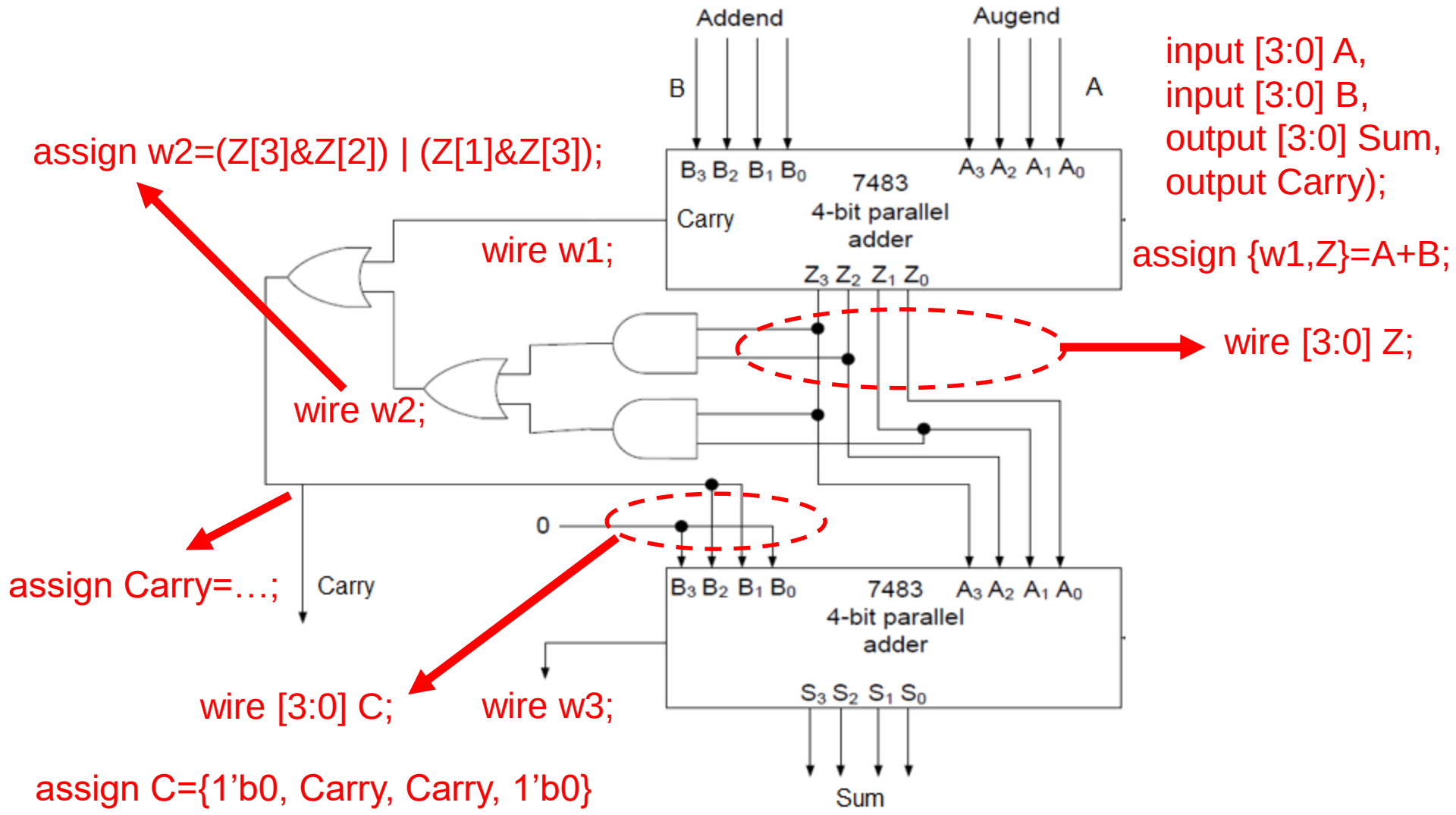

```
module Four_bit_adder(
    input [3:0] A,
    input [3:0] B,
    output [3:0] Sum,
    output Carry );

assign {Carry,Sum}=A+B;

endmodule
```

Remarks

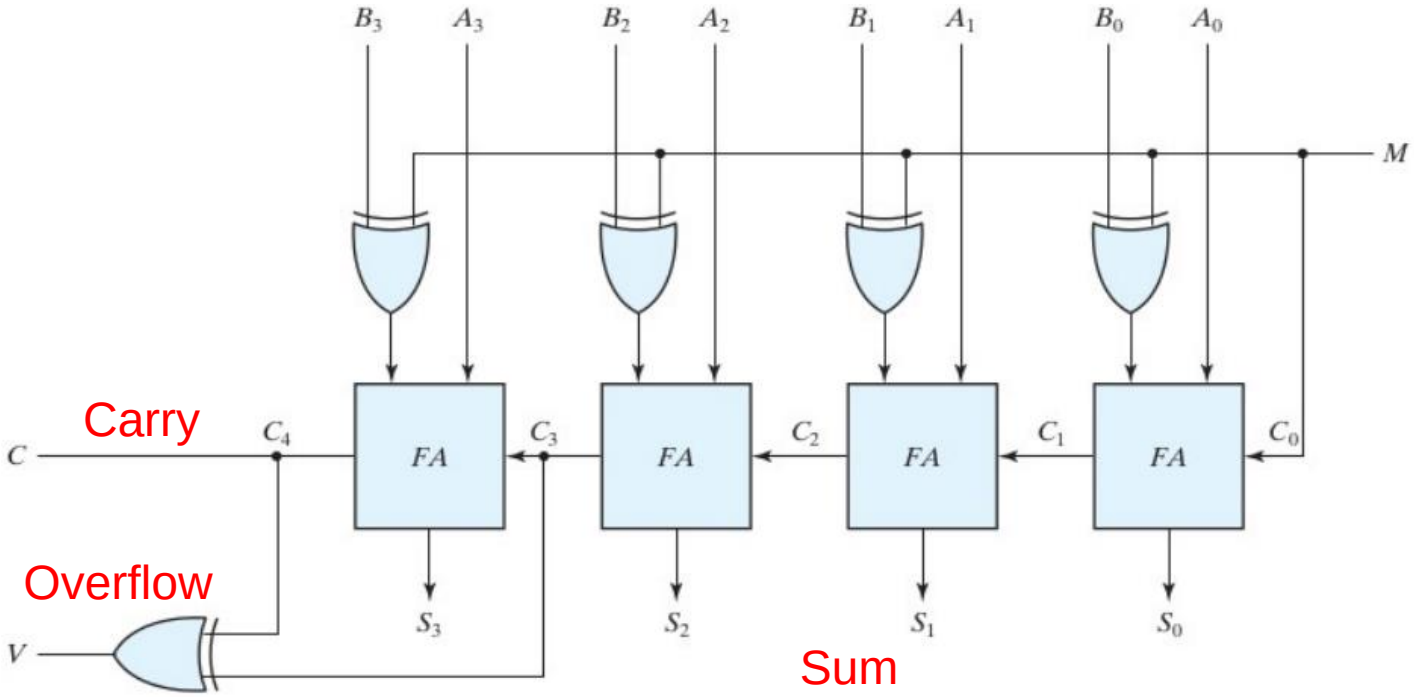
[3:0] [MSB:LSB]

Concatenation

Problem 1: BCD Adder



Additional Home Assignment
4-Bit Adder Subtractor




```
input [3:0] A,
input [3:0] B,
input M,
output [3:0] Sum,
output Carry,
output Overflow);
```

```
wire  [3:0] X,Y,Z;
assign   X= A&7;  \\ (A& 4'b0111)
assign   Y= (B^{M,M,M,M})&7;
assign  Z=X+Y+M;
assign  Overflow=Carry^Z[3];
```

```
assign {Carry,Sum} = A+(B^{M,M,M,M})+M;
```

Demonstration