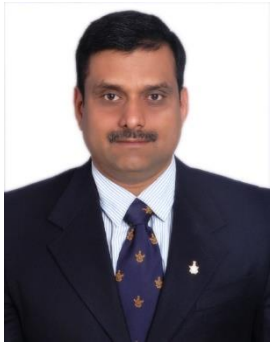
BITS Pilani
Hyderabad Campus
Department of Electrical Engineering

Digital Design : 2020-21
Lab 5
Dataflow Modelling
Implementation of Adders in Xilinx ISE

By Dr. Sanjay Vidhyadharan



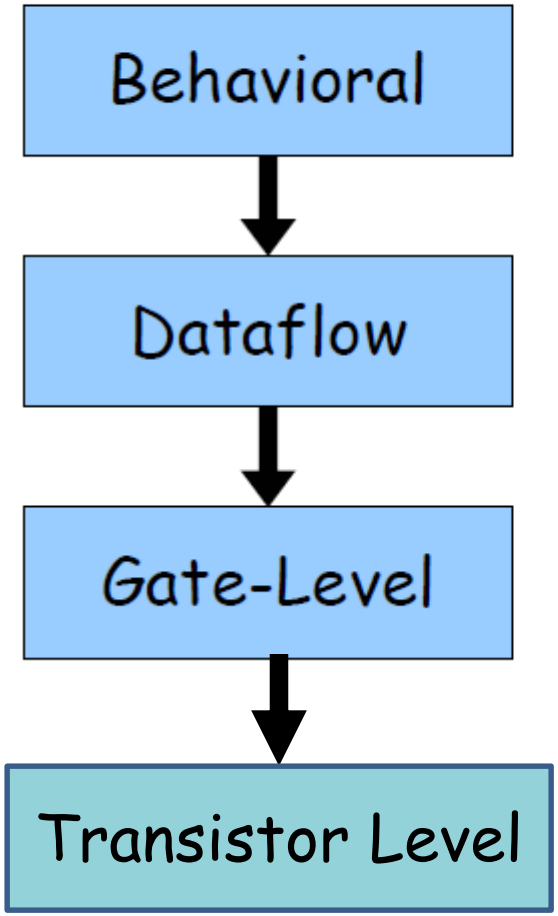
New Concepts

1. Dataflow Modelling

2. Initialization

VLSI Design Levels

Common Abstraction Levels



Module's high-level algorithm is implemented with little concern for the actual hardware

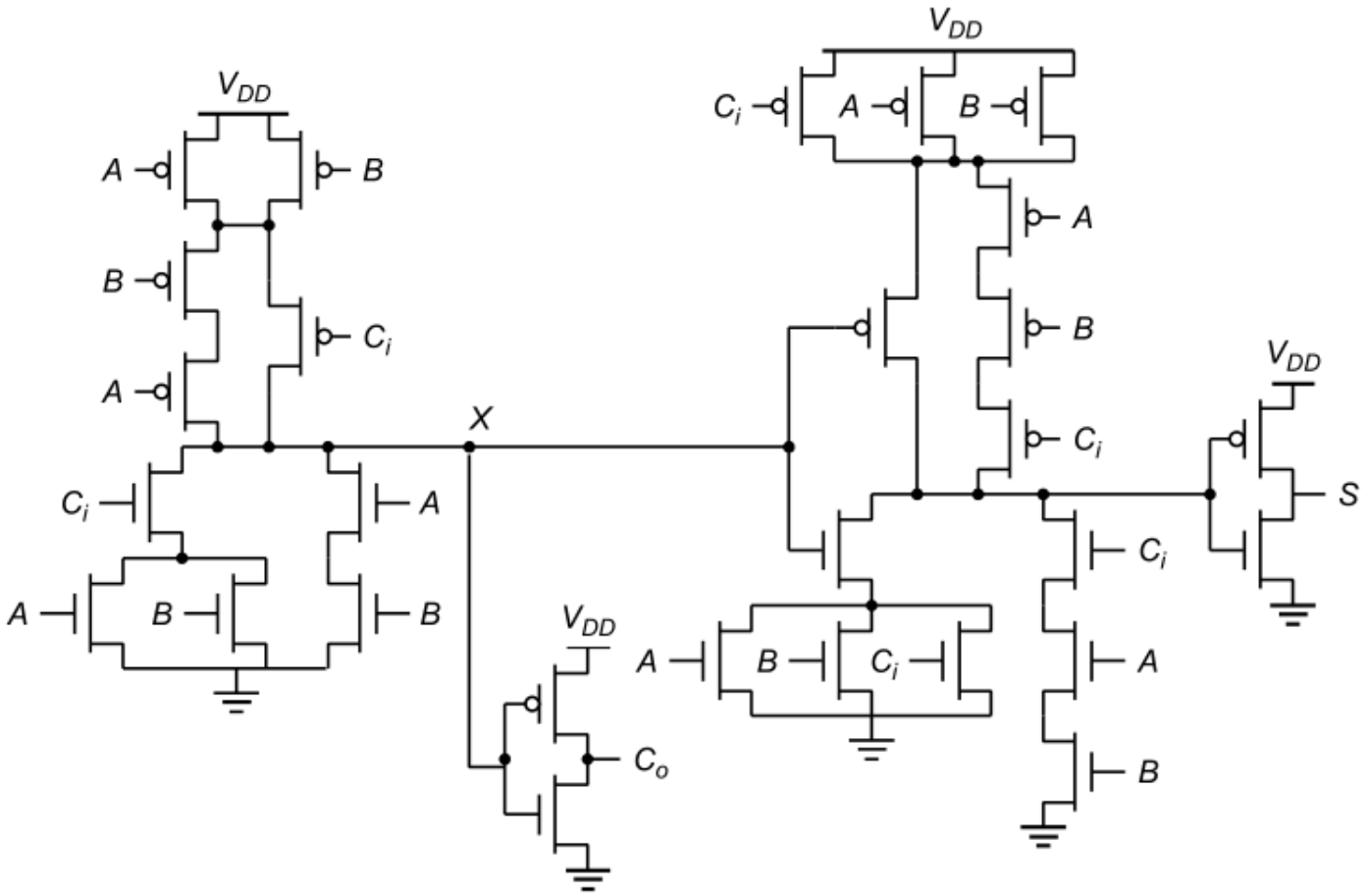
Module is implemented by specifying how data flows between registers

Module is implemented in terms of concrete logic gates (AND, OR, NOT) and their interconnections

Full Custom

BITS Pilani
Hyderabad Campus

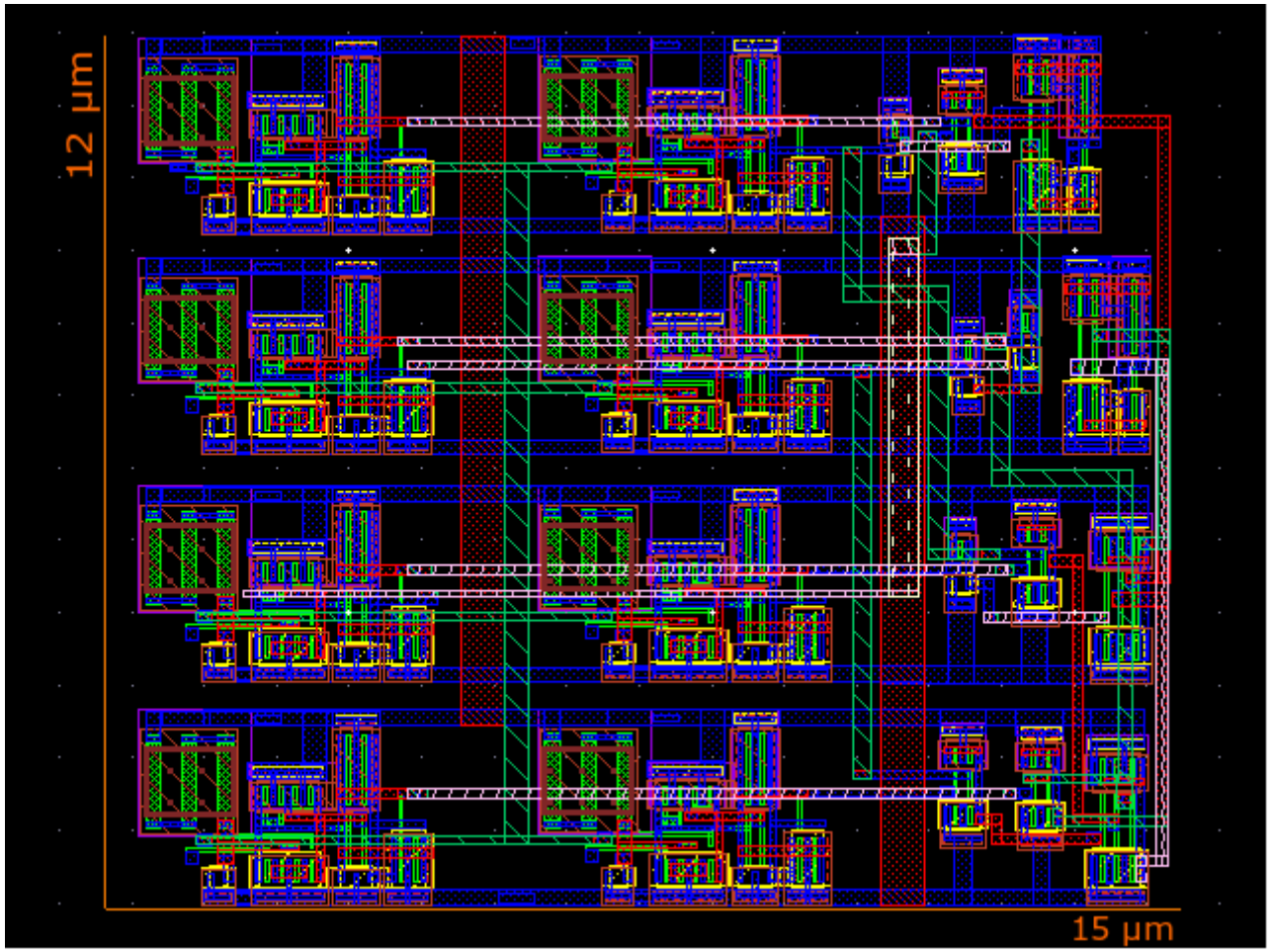
Transistor Level



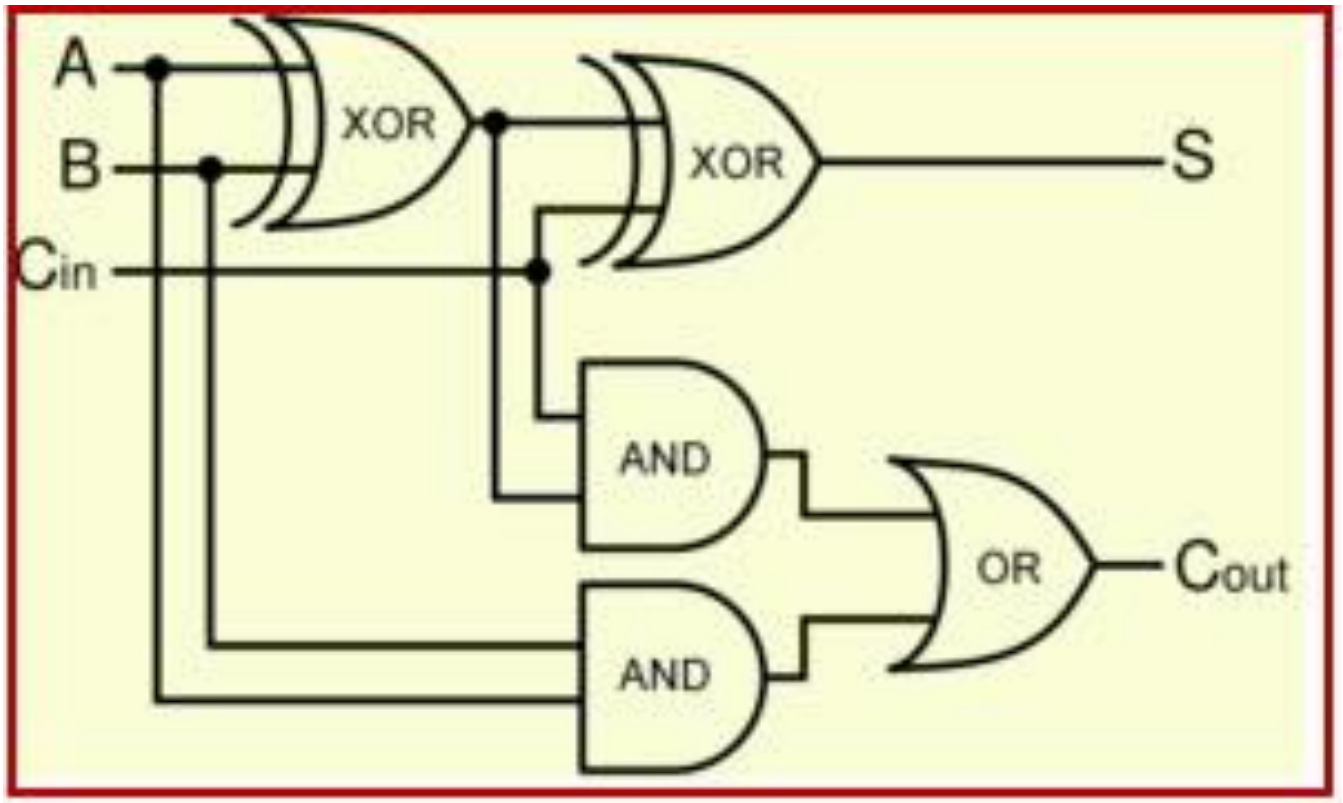
28 Transistors

BITS Pilani
Hyderabad Campus

Transistor Level

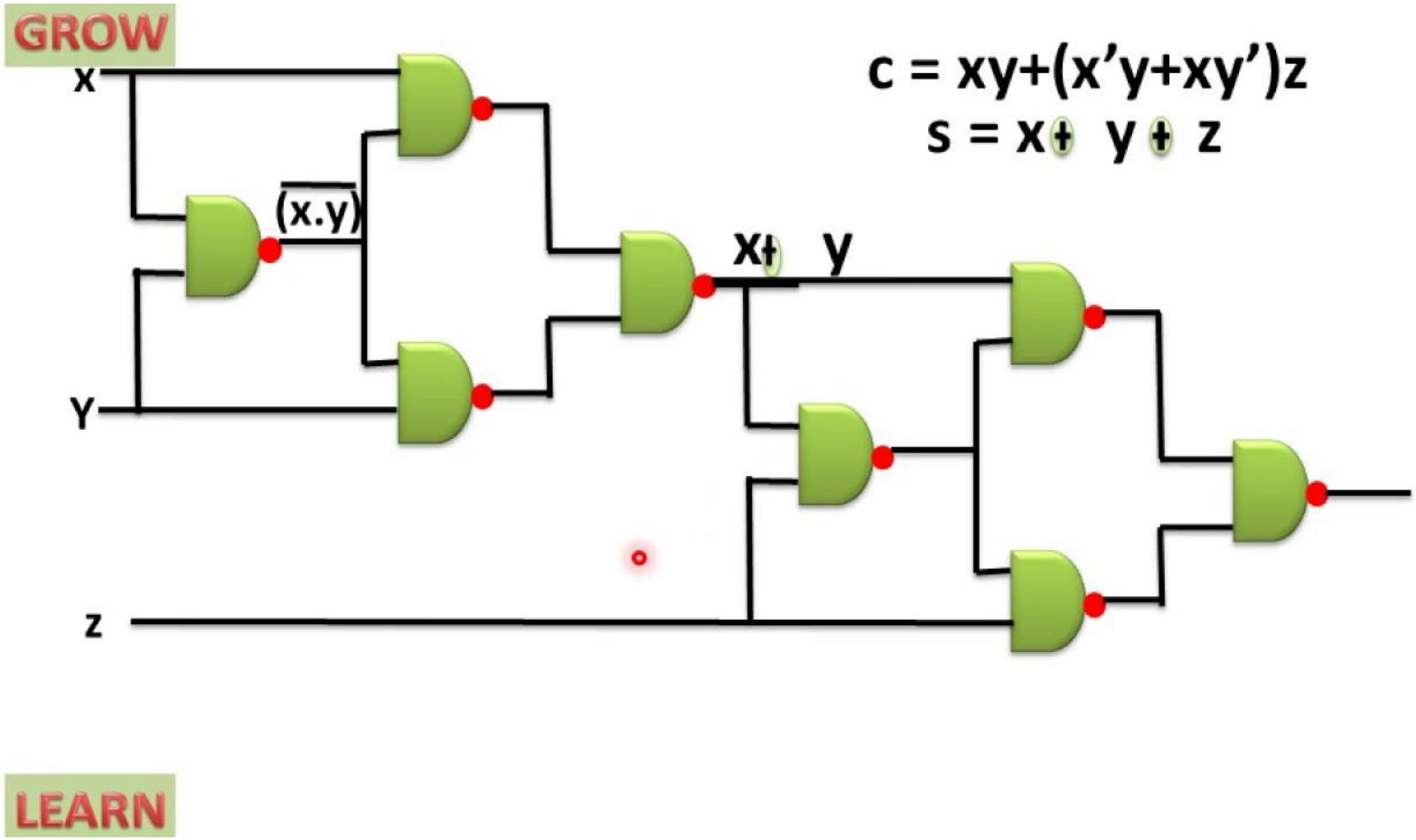


Gate Level Design



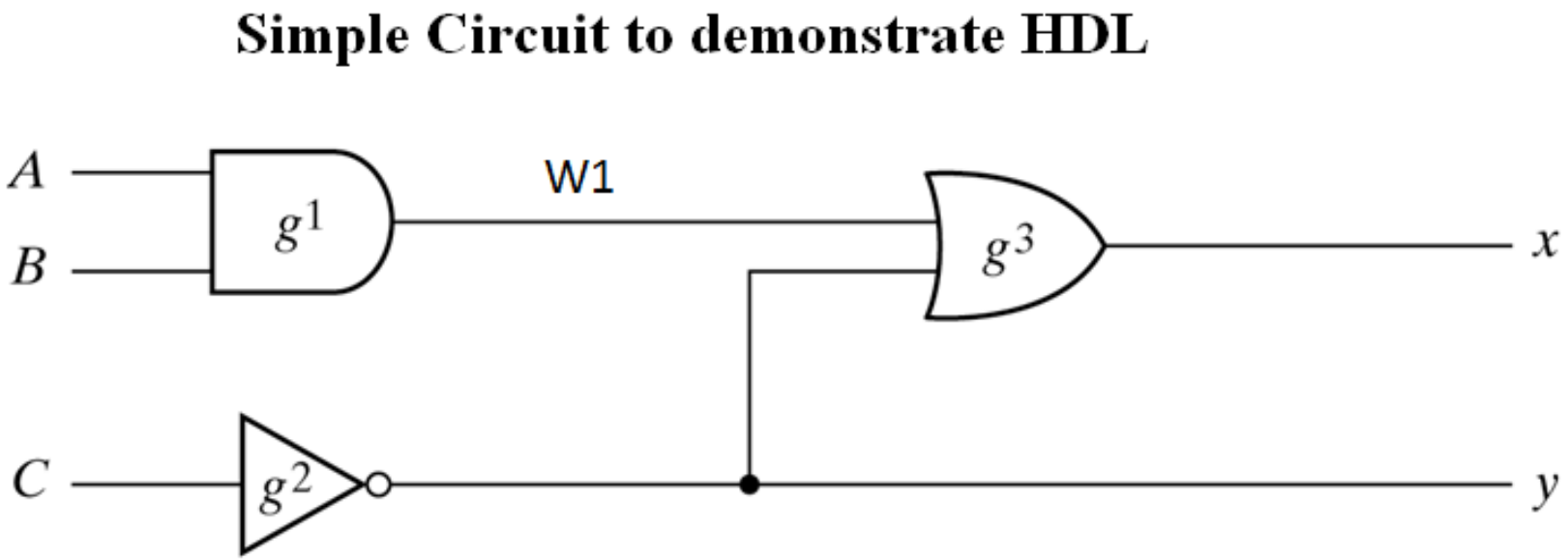
34 Transistors

Dataflow Design



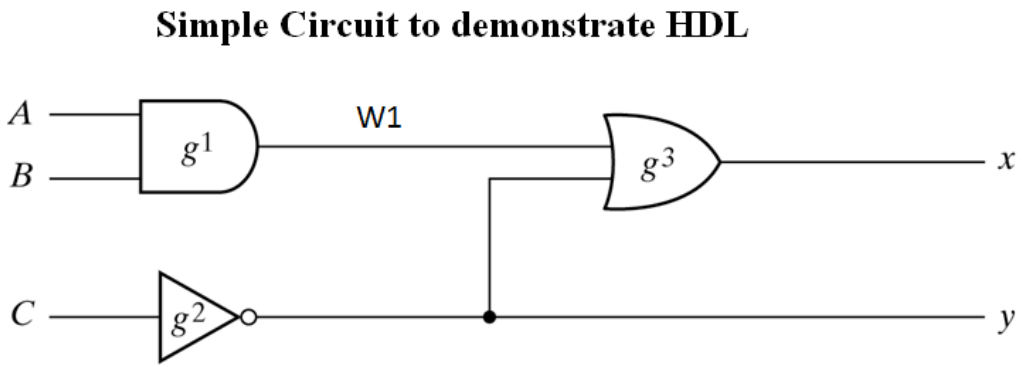
Simple Circuit for Demonstration

Gate Level Modelling



Simple Circuit for Demonstration

Dataflow Modelling




```
module   Simple_circuit (input A,B,C, output x,y);

assign y=~C;
assign x=(A&B)|y;

endmodule
```

Simple Circuit for Demonstration

Verilog operators

Operator Token	Operator name
~	Bitwise negation (unary)
&	Bitwise and (binary)
&~	Bitwise nand (binary)
|	Bitwise or (binary)
|~	Bitwise nor (binary)
^	Bitwise exclusive or (binary
^~ , ~^	Bitwise exclusive nor (binary)

Simple Circuit for Demonstration

Initialization:

$F=(AB+\bar{C}).(CD+\bar{E})$

```
module    Simple_circuit (input A, input B,
input C, output x, output y);
wire      w1;
and       g1 (w1,A,B); // and gate instance
not       g2 (y,C);
or        g3 (x,w1,y);
endmodule
```

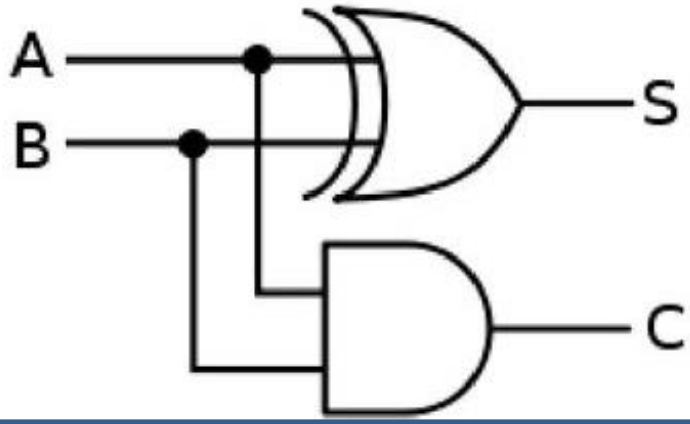
Gate level modeling

```
module   Simple_circuit2 (input A,B,C,D,E output F);
wire      w1,w2,w3,w4;

Simple_circuit g1 (A,B,C,w1,w2);
Simple_circuit g2 (C,D,E,w3,w4);
and  g3 (F,w1,w3);

endmodule
```

Problem Definition

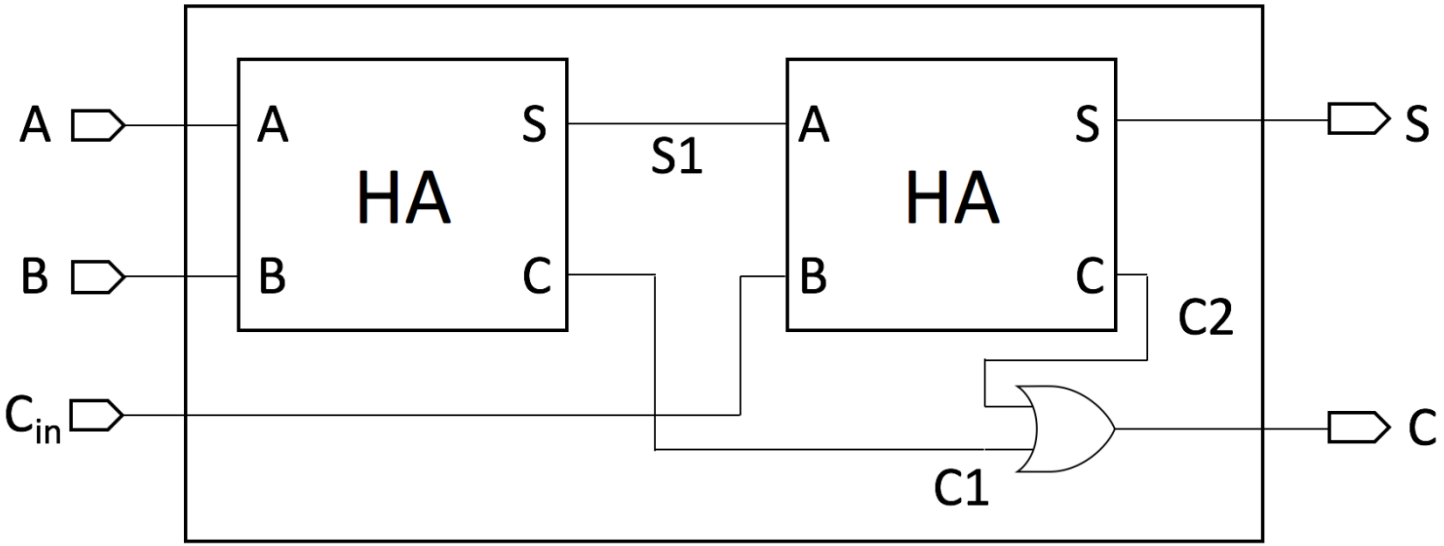
1. Half Adder with dataflow modelling

```
module ha(
    input a, b,
    output c, s
     );

assign
assign
endmodule
```



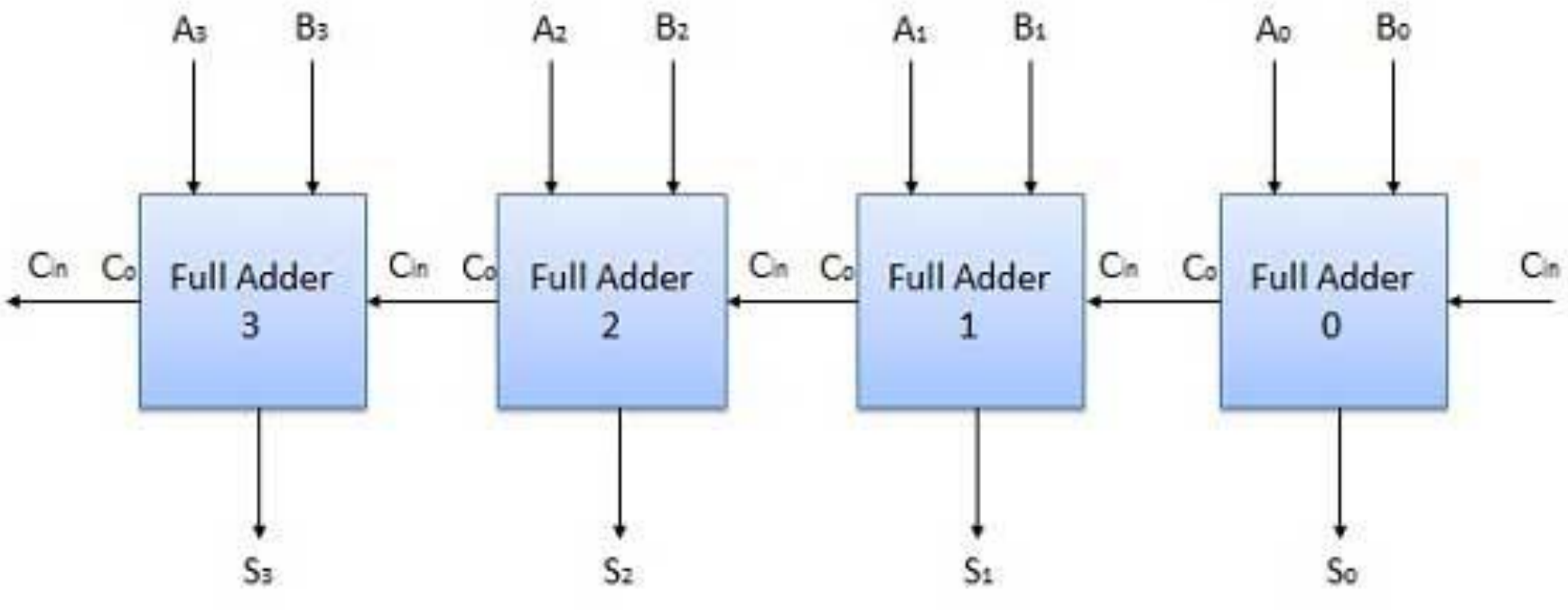
Problem Definition

2. Full Adder using Half Adder with Gate level modeling



Home Assignment

4-bit Parallel Adder



Demonstration