MPI Tutorial-9

8086 Memory Organisation and Interrupts

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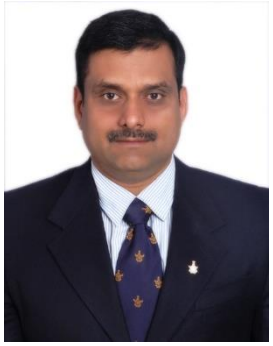


Problem-1

- How many address and data lines are required for the following memory chips?
- 256 X 4
- 1K X 8
- 32K X 16
- Suppose the memory chips are now of size 16K X 8. How should the memory be organized for the third case.

Problem-1

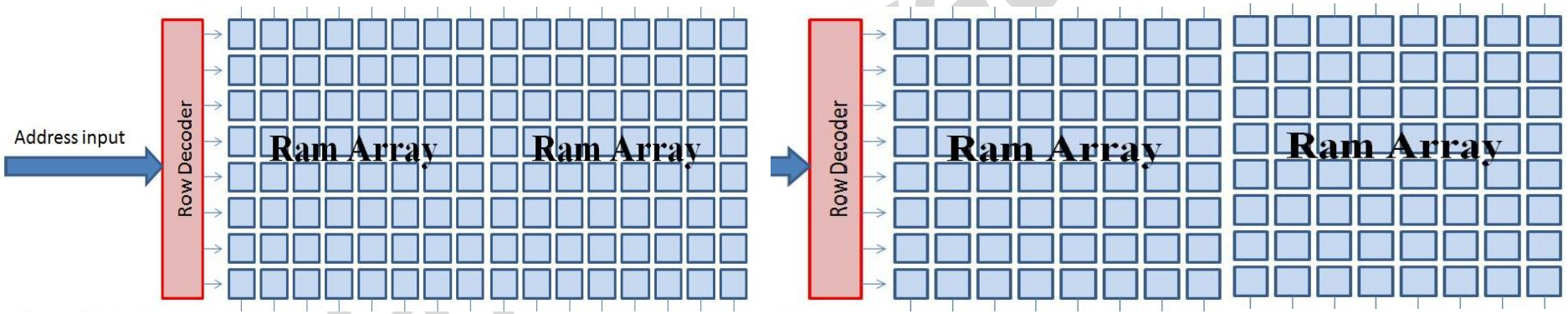
Solution:

- The number of address and data lines required are:
- 256 X 4 : 8 and 4
- 1K X 8 : 10 and 8
- 32K X 16 : 15 and 16

Problem-1

Solution:

Now we need to realize a 32KX16 memory using 16KX8 memory chips. Therefore, we would be needing 4 memory chips of 16KX8 arranged as even and odd memory banks. That is 16KX16 can be realized using using 2 16KX8 where one word of 16 bits can be mapped into even and odd bank address space, respectively.



Problem-2

(i)How many hardware interrupts are there in 8086?

a)2 b)3

c)1 d)4

(ii) Which interrupt has the highest priority?

a)TRAP b)INTR

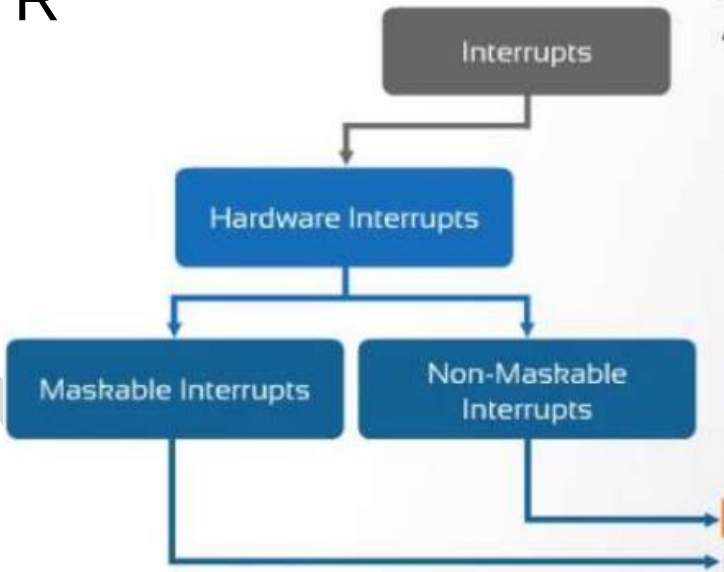
c) INTO d)NMI

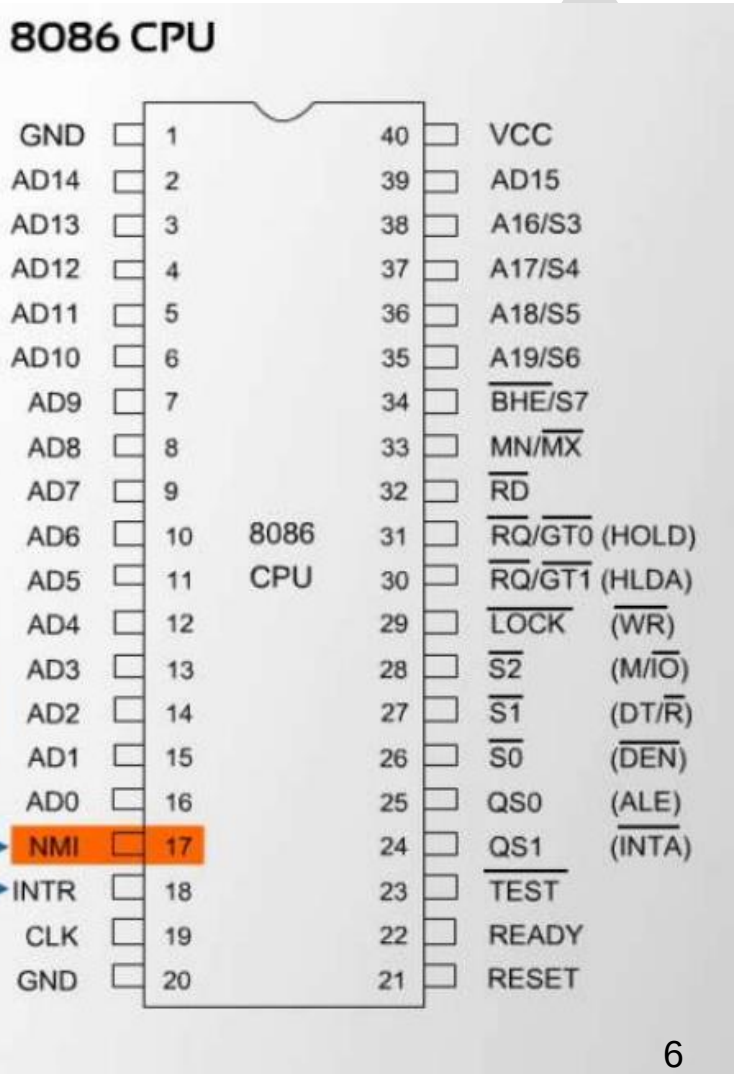
Problem-2

Solution:

(i) 2 hardware interrupts. NMI and INTR

(ii) NMI





Problem-3

What are the Operations performed by IRET and which flags are affected?

Problem-3

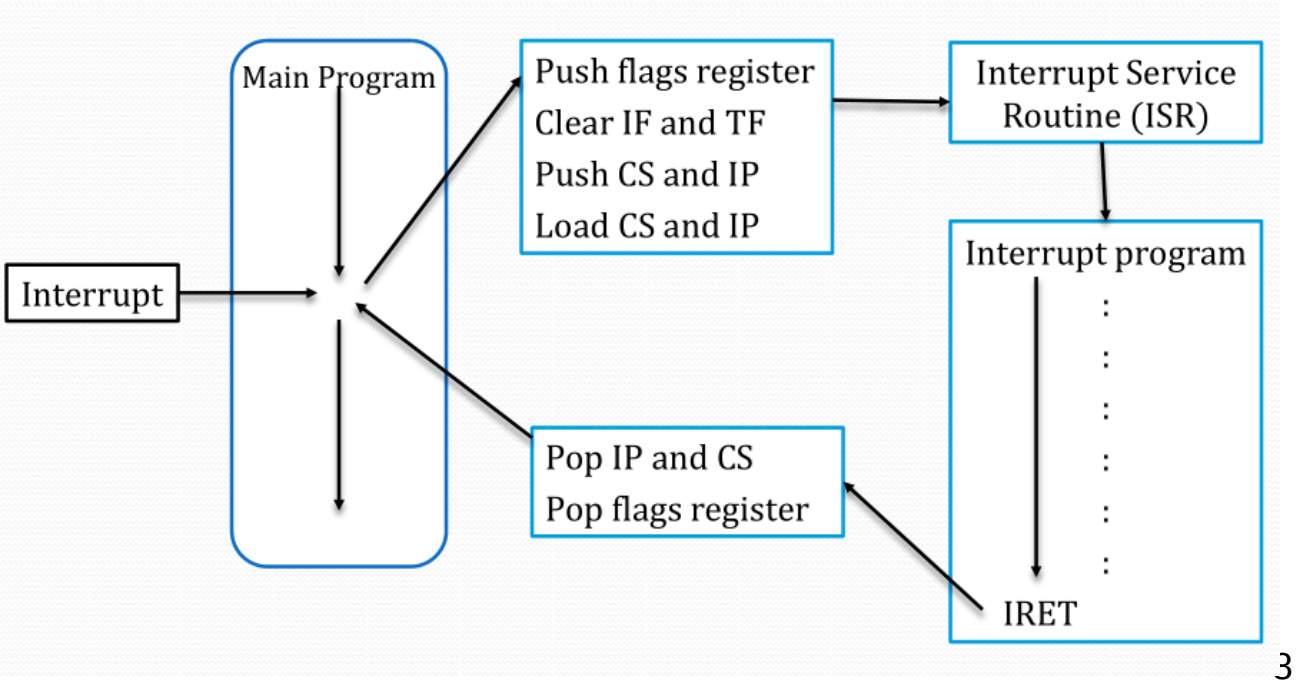
Solution:

[SP]->IP

[SP+2]-> CS

[SP)+4]-> (Flags)

All flags are affected.



Problem-4

(i) Mention the address at which $CS_{40}\ and\ IP_{40}$ corresponding to the vector 40 would be stored in memory?

(ii) Mention five dedicated interrupt types and their purpose?

Problem-4

Solution

(i) INT 40, for its storage, requires four memory locations

Two for IP40 and two for CS40.

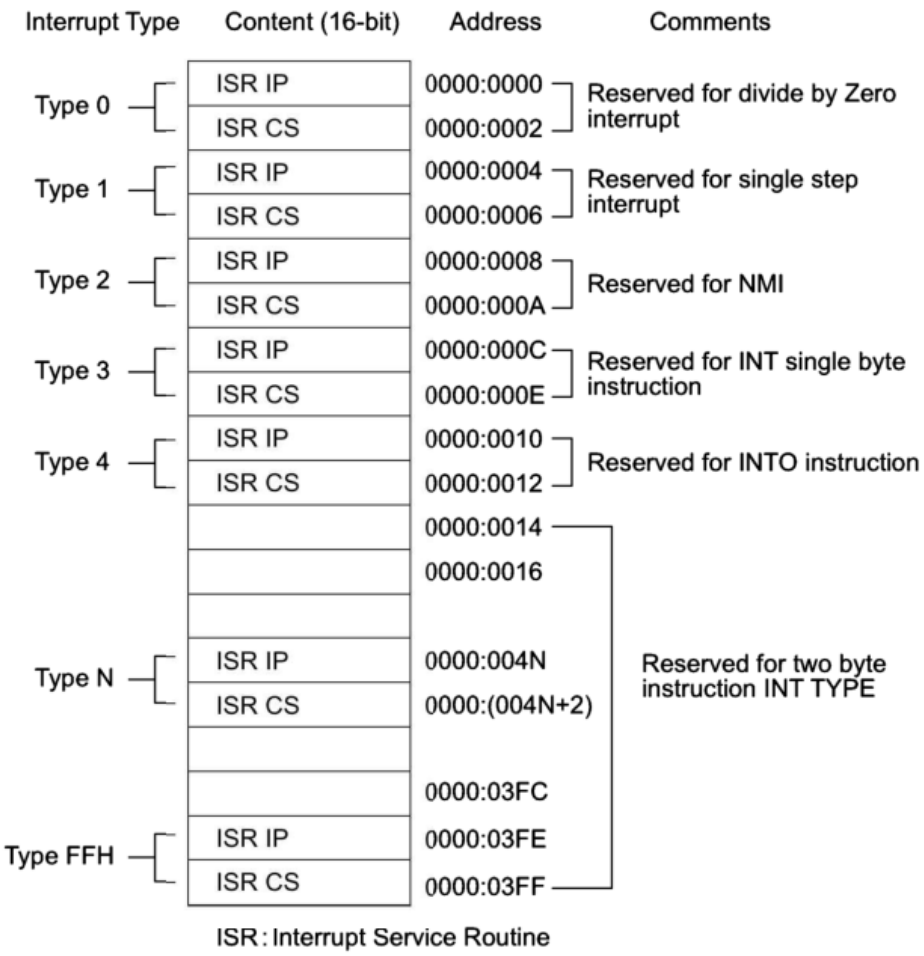
The addresses are calculated as follows:

$4 \times 40 = (160)_{10} = (1010\ 0000)_2 = A0H.$

Thus, IP40 is stored starting at 000A0 H and CS40 is stored starting at 000A2 H.

(ii)

Interrupt type	Purpose
0	Divide error
1	Single step
2	Non-maskable Interrupt
3	Break point
4	Overflow



Problem-4

Solution

(ii)

Interrupt type	Purpose
0	Divide error (Called Automatically)
1	Single step

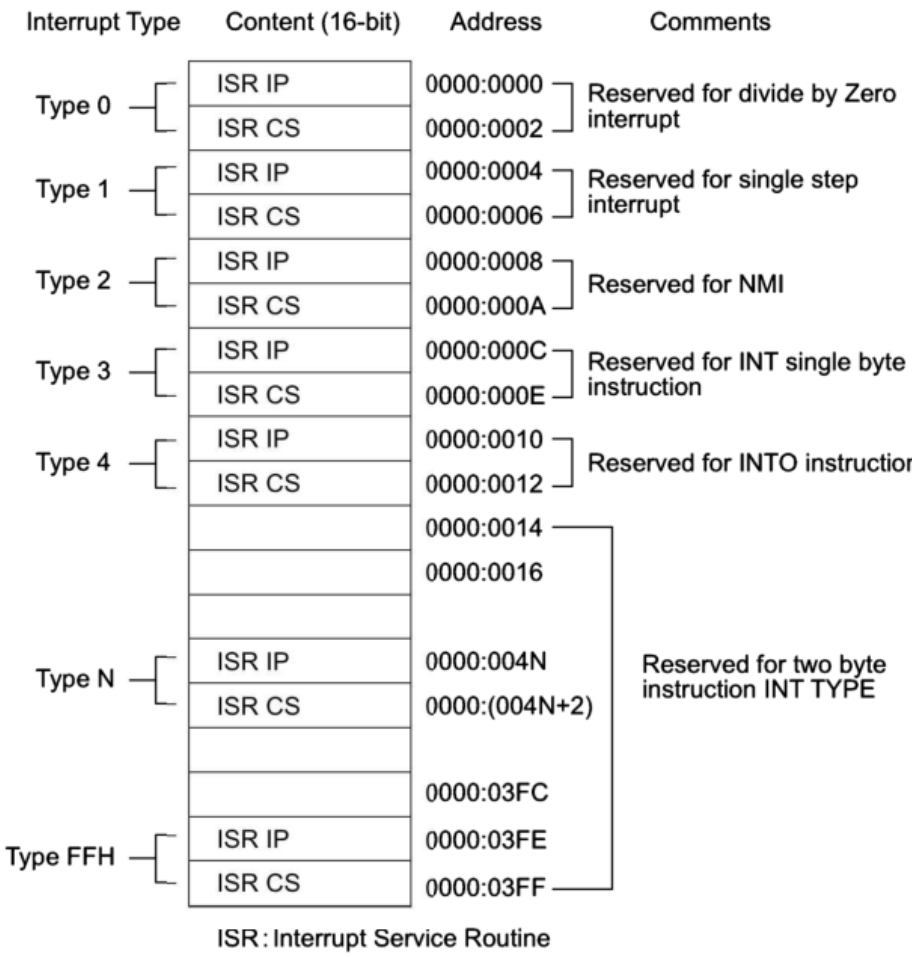
```
PUSHF ;
MOV BP, SP
OR  [ BP ], 0100H ;
POPF
```

To reset the trap flag

AND [BP], OFEFFH instruction instea

OR [BP], 0100H.

2	Non-maskable Interrupt (NMI PIN)
3	Break point
4	Overflow (Not Called Automatically)



Problem-5

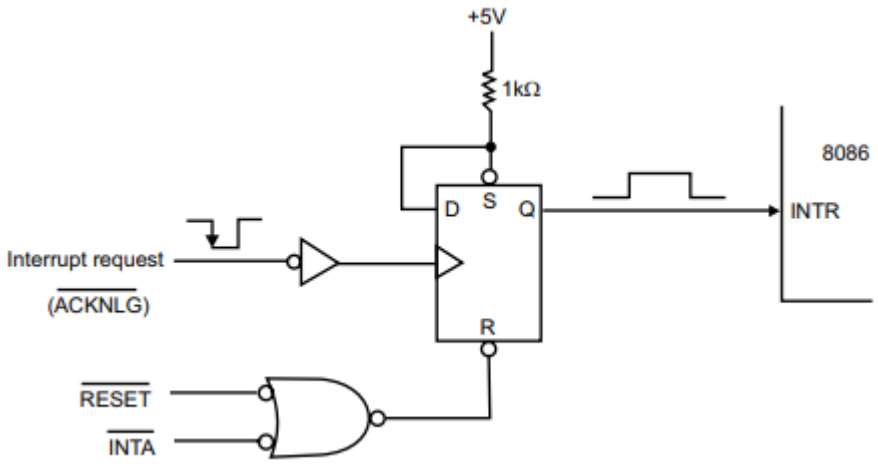
Draw a circuit that will terminate the INTR when interrupt request has been acknowledged.

Problem-5

Solution:

The figure below makes INTR input of 8086 to go into 1 state once the interrupt request comes from some external agency. The falling edge of the peripheral clocks the flip-flop which makes INTR to become 1.

The first $\overline{INTR}$ pulse then resets Q, making INTR to become 0. This ensures that no second interrupt request is recognized by the system. The reset input sees to it that INTR remains in the 0 state when the system is reset.



Thank You