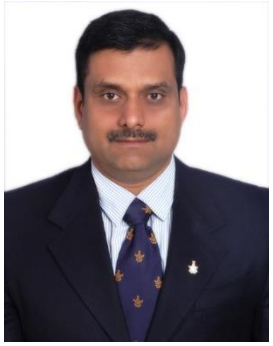
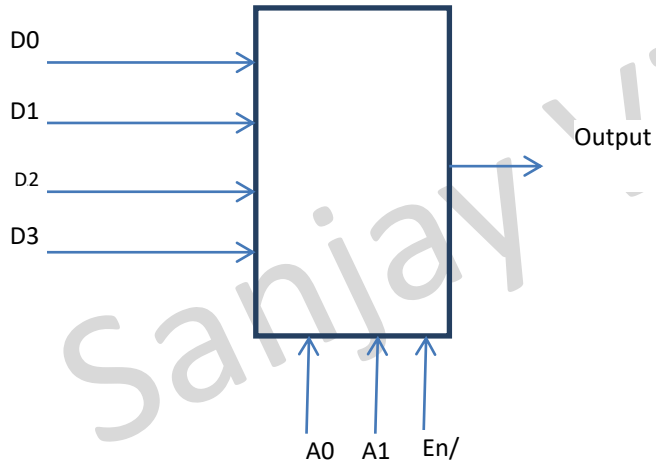
Microprocessors and Interfaces: 2021-22
Tut-2
Microprocessor Design

By Dr. Sanjay Vidhyadharan



Problem-1

The output of below block is driven by 4 inputs. All the inputs and output are 1 bit width. The selection of the input is done by the two address bits A0 and A1 and En/ as per truth table given below. Design the block using logic gates



A1	A0	En/	Output
x	x	1	High Imp
0	0	0	D0
0	1	0	D1
1	0	0	D2
1	1	0	D3

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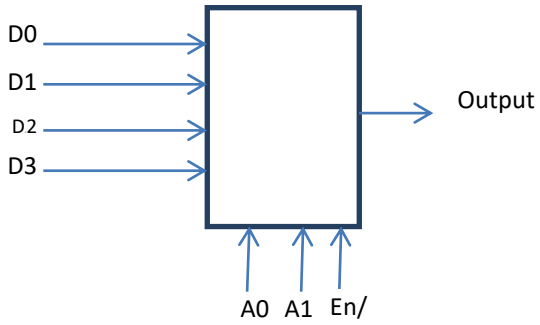
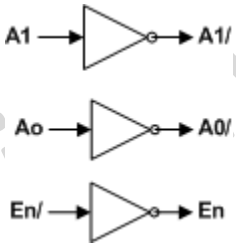
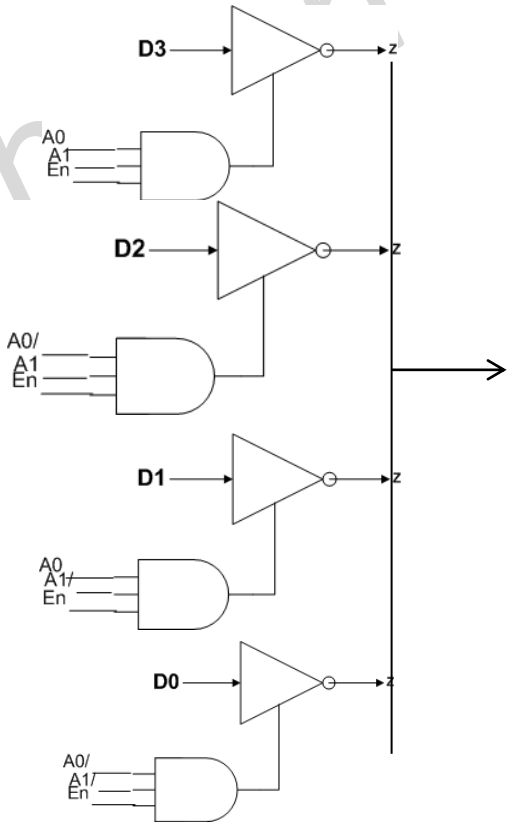
Problem-1

Solution:







A1	A0	En/	Output
x	x	1	High Imp
0	0	0	D0
0	1	0	D1
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1	1	0	D3

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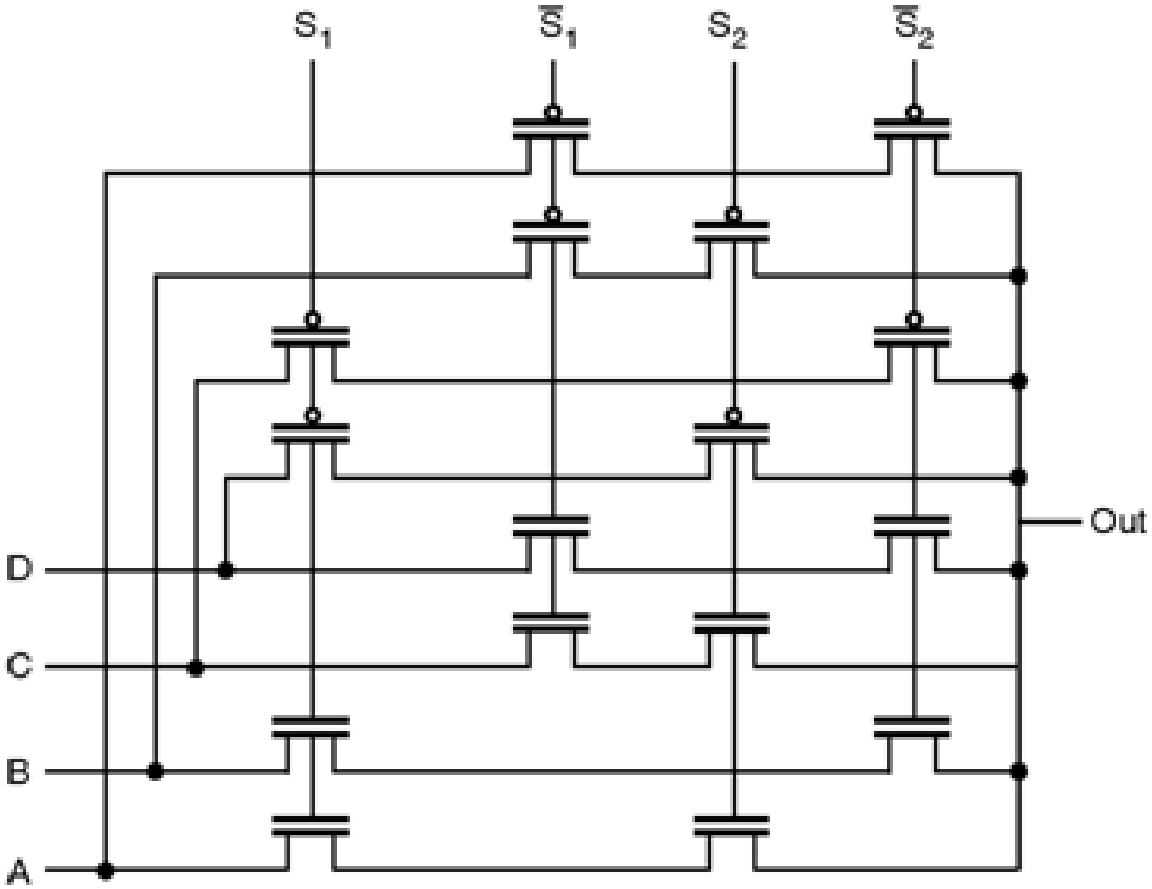
Practical Muxs



4 : 1 MUX using CMOS logic

Problem-2

A relay is to be operated whenever X or Y is true. X is selected if EnX is true and Y is selected if EnY is true. At any time only EnX or EnY only will be true. The relay needs 20 mA to be operated. Design the circuit to do this function.

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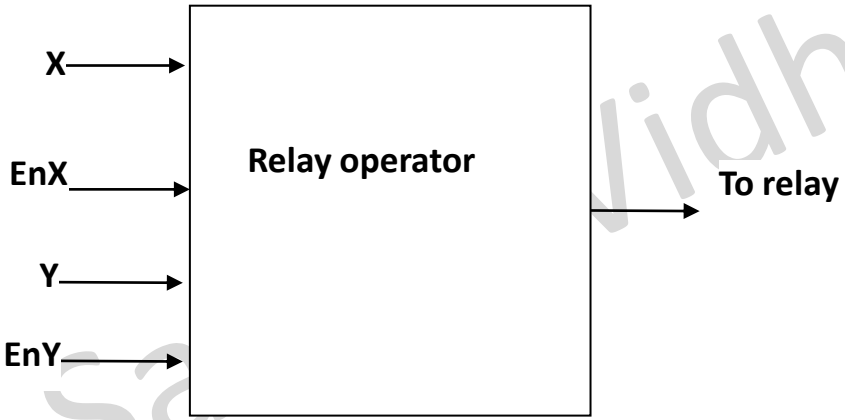
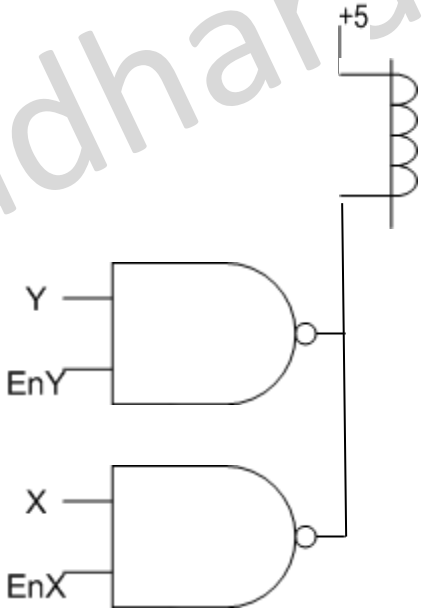
Problem-2

Solution





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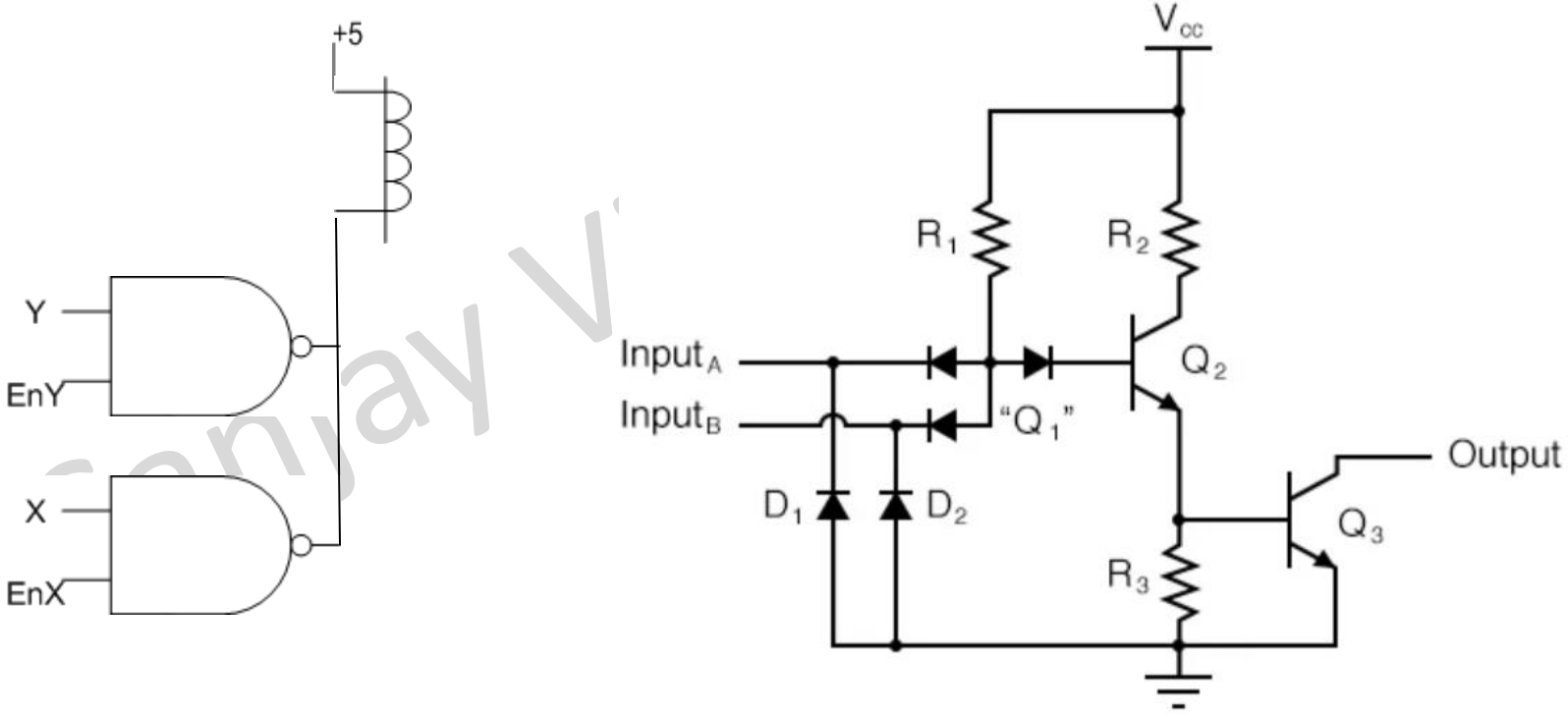
Problem-2

Solution



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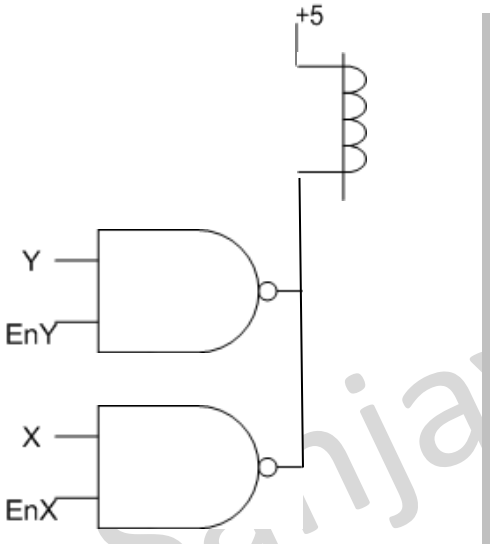
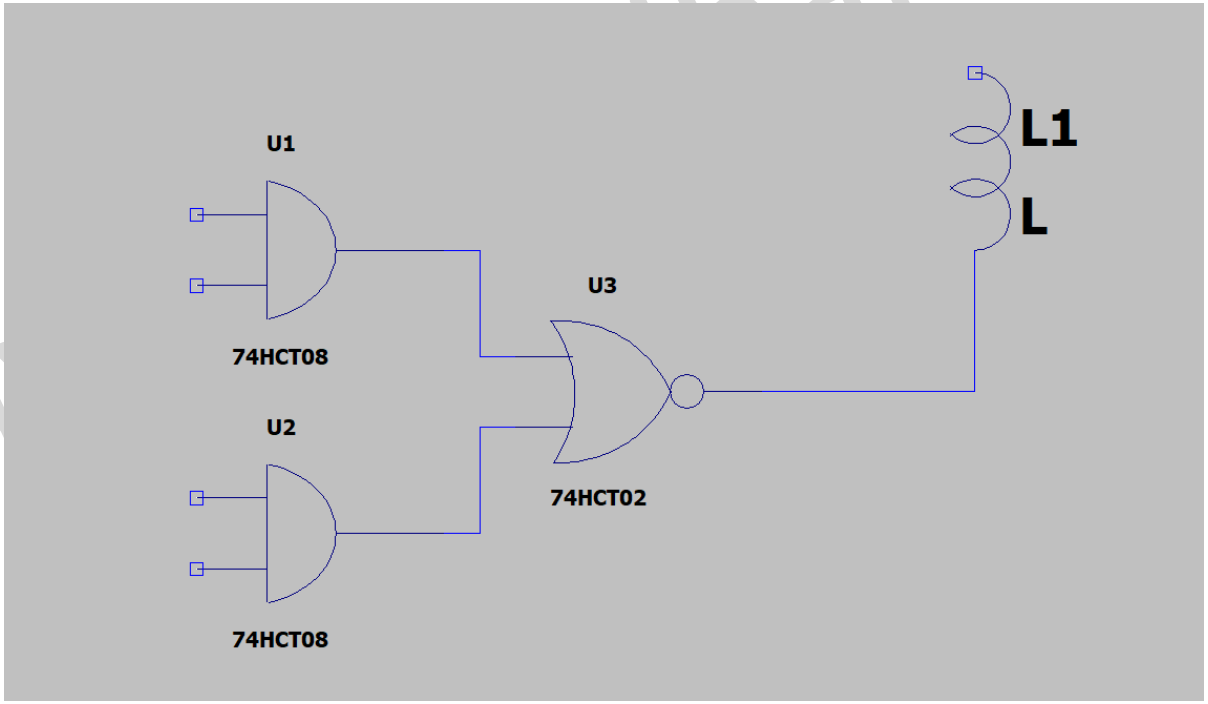
Problem-2

Solution





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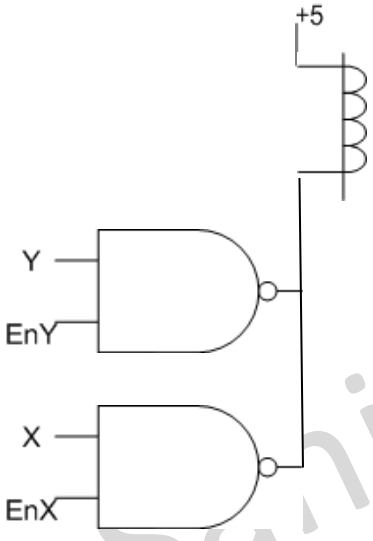
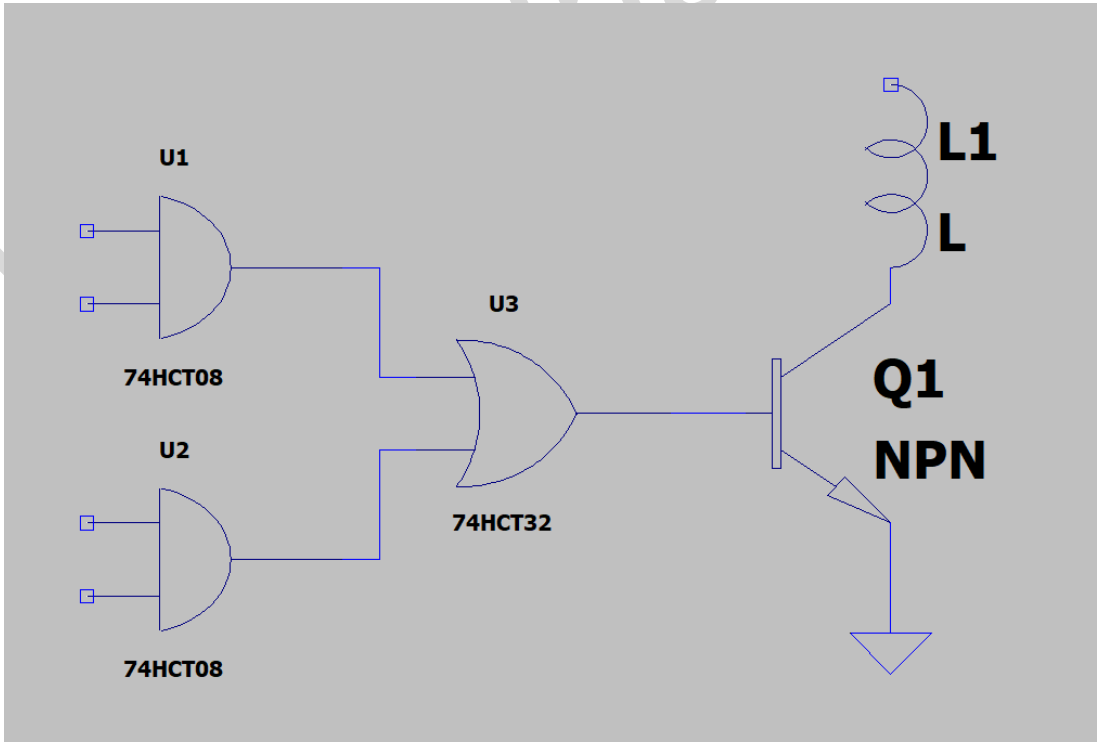
Problem-2

Solution





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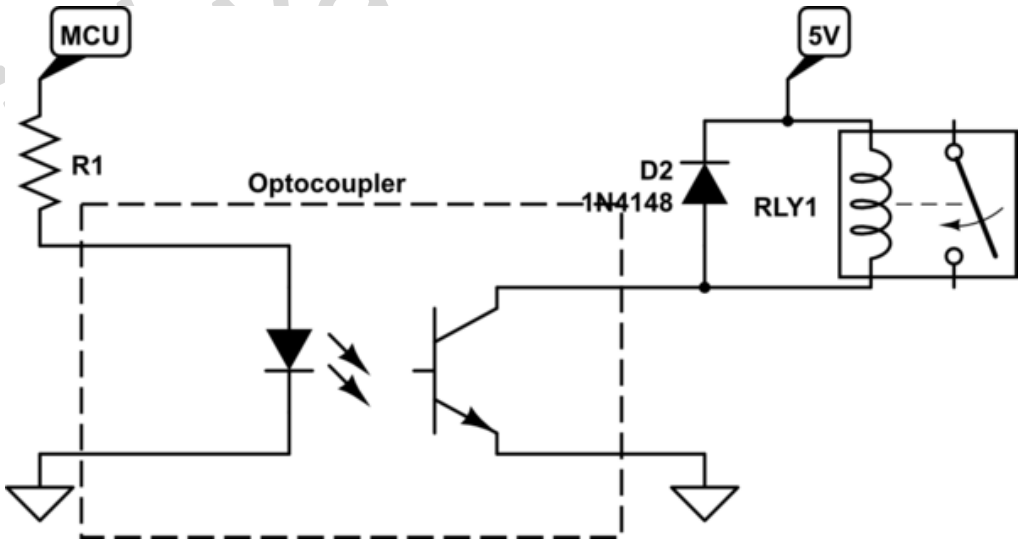
Problem-2

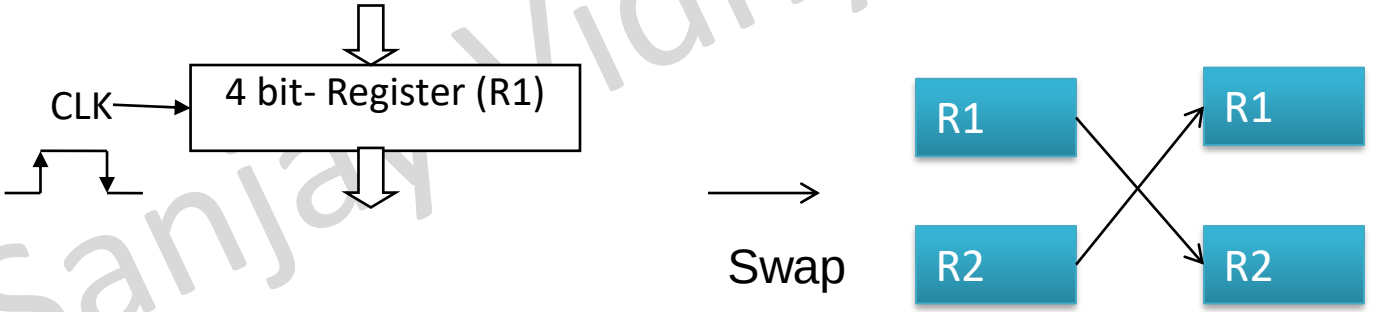
Solution



Subramaniyadharan

Problem-3

The content of two 4 bit registers is to be swapped. The behavior of the register is as below: The register is 4 bit wide. When a clock pulse is applied at CLK the input get stored in the register and is available as output after 1 msec of the rising edge of the clock.



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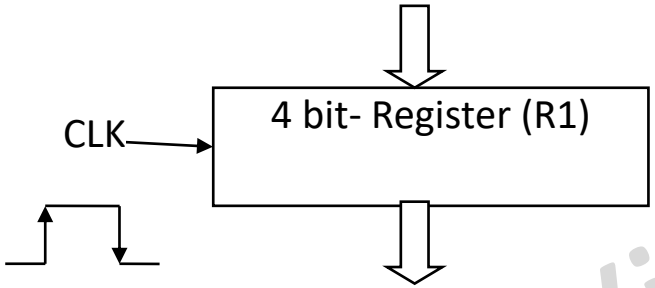
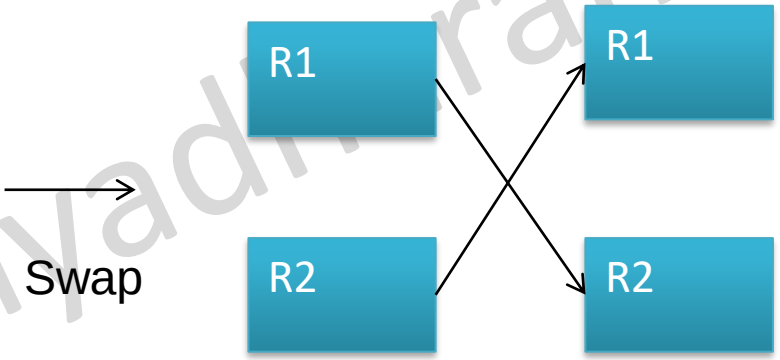
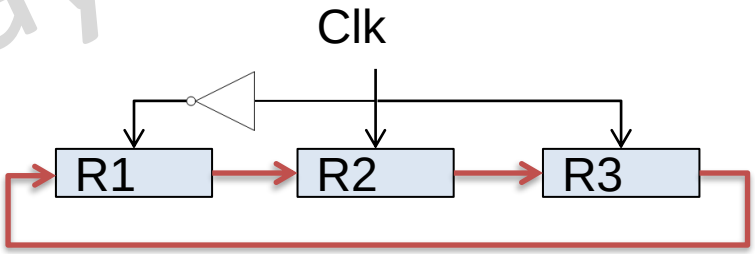
Problem-3

Solution







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Problem-4

Three are 3 registers of 4 bit width A, B and C. The majority logic circuit , shown as a block below outputs the majority value if two or more inputs are same. Ex: If A=5, B=5, C=7; Output will be 5. Output will be in high impedance state if all are of different values. Design the logic using logic gates. Or use any standard building blocks like comparators.

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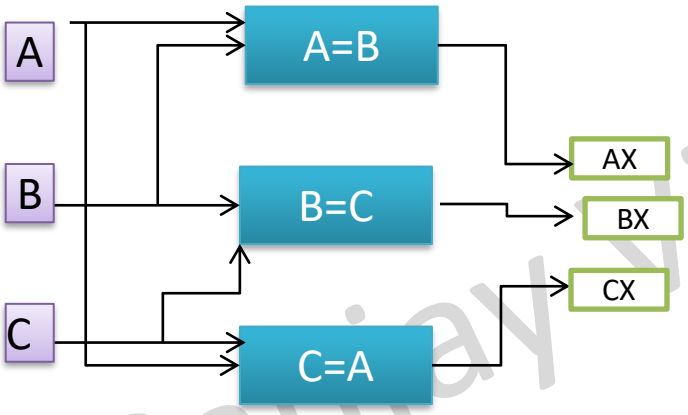
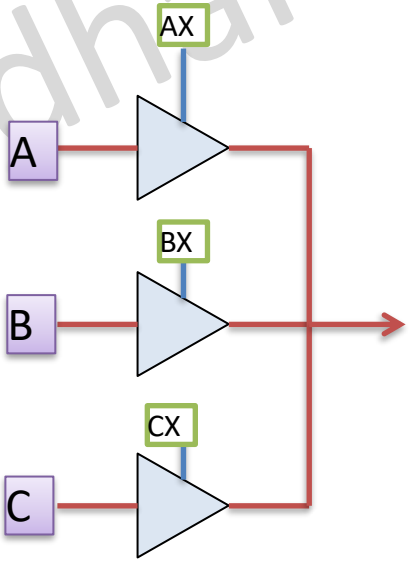
Problem-4

Solution





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Problem-5

- Consider a system having 14 bit address with 16 bits of register. The main memory is byte addressable with an access time of 1ns. How many data lines will be present? If the data bus is of 8bits, what is the time that will be required to load a register? What is the time that will be required if the data bus is 16 bits?

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Problem-5

- Consider a system having 14 bit address with 16 bits of register. The main memory is byte addressable with an access time of 1ns. How many data lines will be present? If the data bus is of 8bits, what is the time that will be required to load a register? What is the time that will be required if the data bus is 16 bits?

Solution

- No. of data lines=2^14.
- If data bus is 8 bits, 16bits can transferred as chunks of two 8-bits at a time. Therefore, total time is 2ns (ignoring other overheads).
- Since data bus is 16bits, time required now will be 1ns (ignoring other overheads).

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