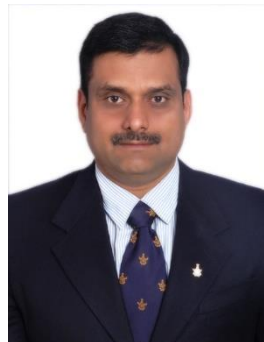




MPI Tutorial-11

Memory Interface

By Dr. Sanjay Vidhyadharan



Question 1

- Design an 8088 based system that has the following memory requirements:
 - 256K of ROM from 00000_{H}
 - 256K of ROM from $\text{C}0000_{\text{H}}$
 - 256K of RAM from 60000_{H}

Available Chips:

64K ROM -8

64K RAM -4

LS138-2

Solution 1

- 256K of ROM from 00000_{H}
- 00000 to $3FFFF_{\text{H}}$
- 256K of ROM from $C0000_{\text{H}}$
- $C0000$ to $FFFFFF_{\text{H}}$
- 256K of RAM from 60000_{H}
 60000 to $9FFFF_{\text{H}}$

Available Chips:

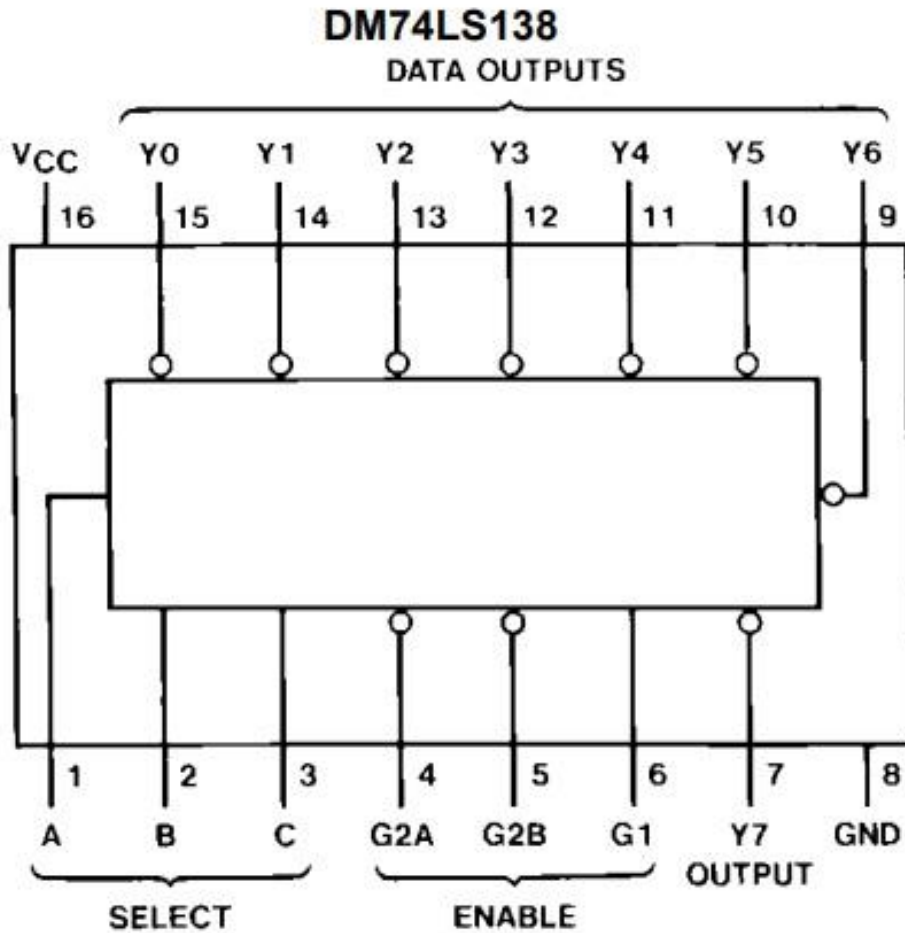
64K ROM -8 --- A_0 - A_{15}

64K RAM -4 --- A_0 - A_{15}

1K	10 Lines
2K	11 Lines
4K	12 Lines
8K	13 Lines
16 K	14 Lines
32 K	15 Lines
64 K	16 Lines
128 K	17 Lines
256 K	18 Lines
512 K	19 Lines
1M	20 Lines

256 K	18 Lines	0011-1111-1111-1111-1111
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Solution 1

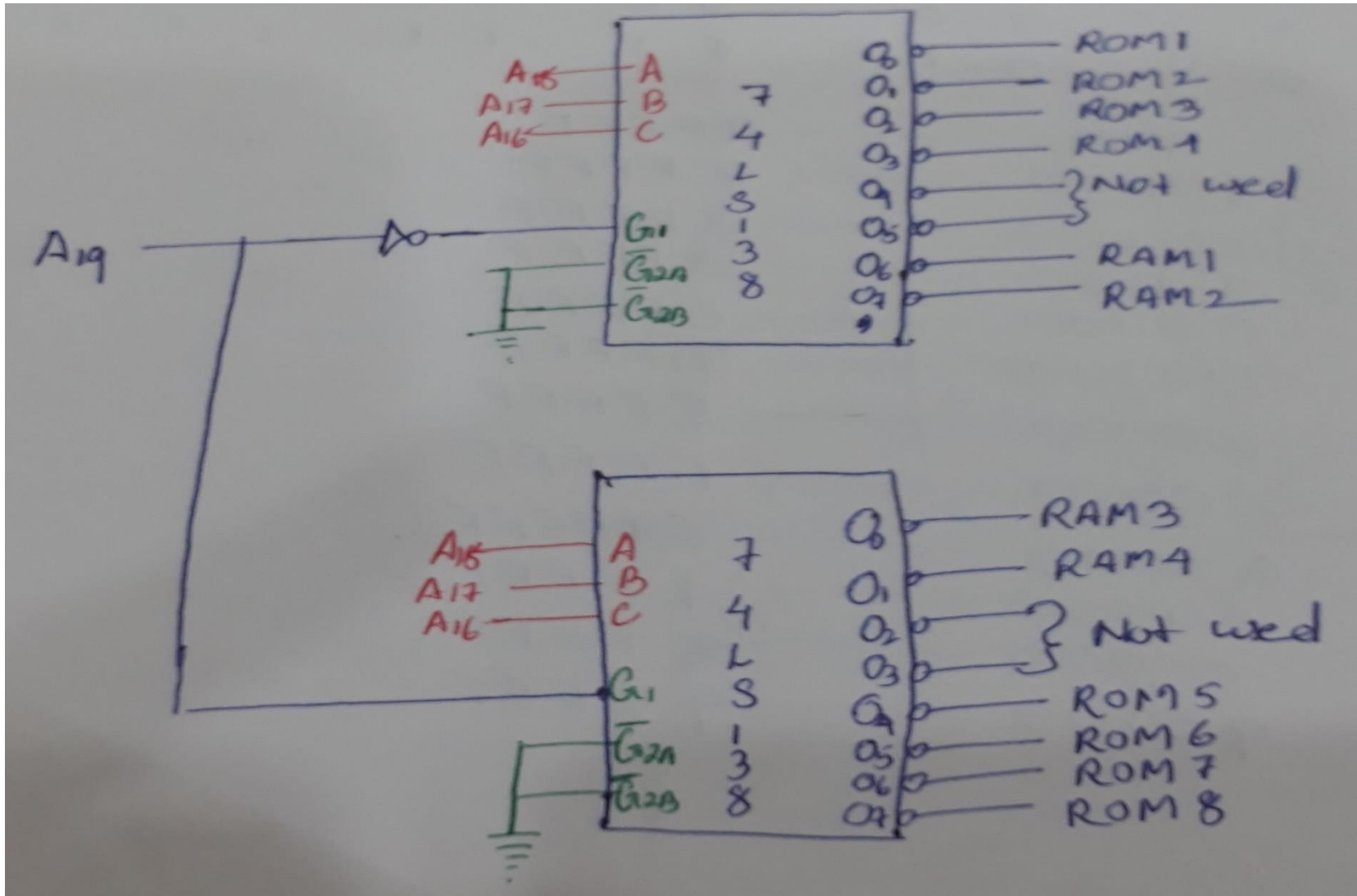


Solution 1

CHIP	A19	A18	A17	A16	DECODE R O/P
ROM1	0	0	0	0	D1 O ₀
ROM2	0	0	0	1	D1 O ₁
ROM3	0	0	1	0	D1 O ₂
ROM4	0	0	1	1	D1 O ₃
RAM1	0	1	1	0	D1 O ₆
RAM2	0	1	1	1	D1 O ₇
RAM3	1	0	0	0	D1 O ₀
RAM4	1	0	0	1	D2 O ₁
ROM5	1	1	0	0	D2 O ₄
ROM6	1	1	0	1	D2 O ₅
ROM7	1	1	1	0	D2 O ₆
ROM8	1	1	1	1	D2 O ₇

LS138-2 -A₁₆-A₁₈ directly connected to decoder A,B,C select lines

Solution 1

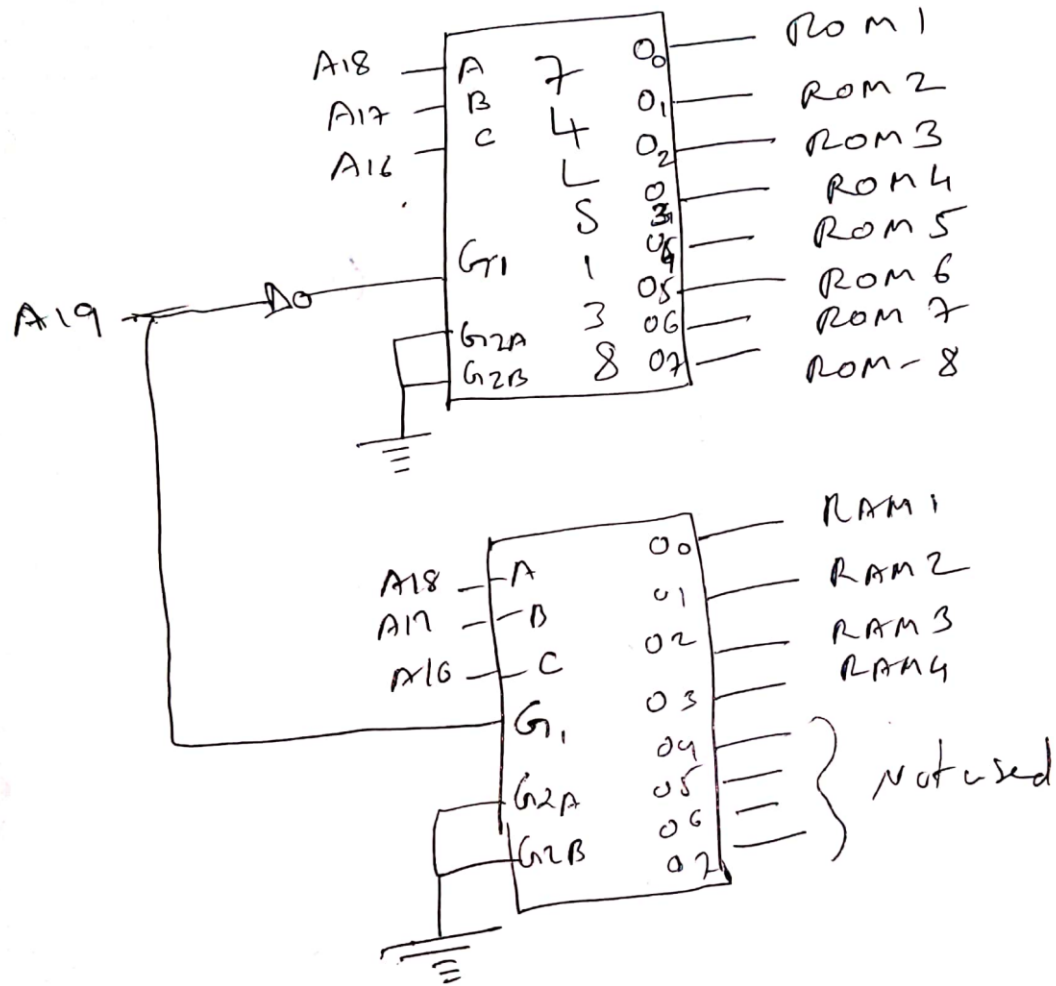


Solution 1

CHIP	A19	A18	A17	A16	DECODE R O/P
ROM1	0	0	0	0	D1 O ₀
ROM2	0	0	0	1	D1 O ₁
ROM3	0	0	1	0	D1 O ₂
ROM4	0	0	1	1	D1 O ₃
ROM5	0	1	0	0	D1 O ₄
ROM6	0	1	0	1	D1 O ₅
ROM7	0	1	1	0	D1 O ₆
ROM8	0	1	1	1	D1 O ₇
RAM1	1	0	0	0	D2 O ₀
RAM2	1	0	0	1	D2 O ₁
RAM3	1	0	1	0	D2 O ₂
RAM4	1	0	1	1	D2 O ₃

LS138-2 -A₁₆-A₁₈ directly connected to decoder A,B,C select lines

Solution 1



Question 2

Design 8088 based system interface with

SRAM: 16 KB From 02000_H

ROM: 16 KB From 09000_H

Memory chips to be used are as per following specification

SRAM- 2K X 8bit

ROM- 2K x 8bit

74138 decoders (4 numbers available)

Using these decoders and minimum number of logic gates
draw the memory interfacing diagram

Solution 2

- 16K of SRAM from 02000_H
- 02000 to 05FFF_H
- 16K of ROM from 09000_H
- 09000 to 0CFFFF_H

Available Chips:

2K ROM -8 ---A₀-A₁₀

2K SRAM -8 ---A₀-A₁₀

1K	10 Lines
2K	11 Lines
4K	12 Lines
8K	13 Lines
16 K	14 Lines
32 K	15 Lines
64 K	16 Lines
128 K	17 Lines
256 K	18 Lines
512 K	19 Lines
1M	20 Lines

16 K	14 Lines	0000-0011-1111-1111-1111
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Solution 2

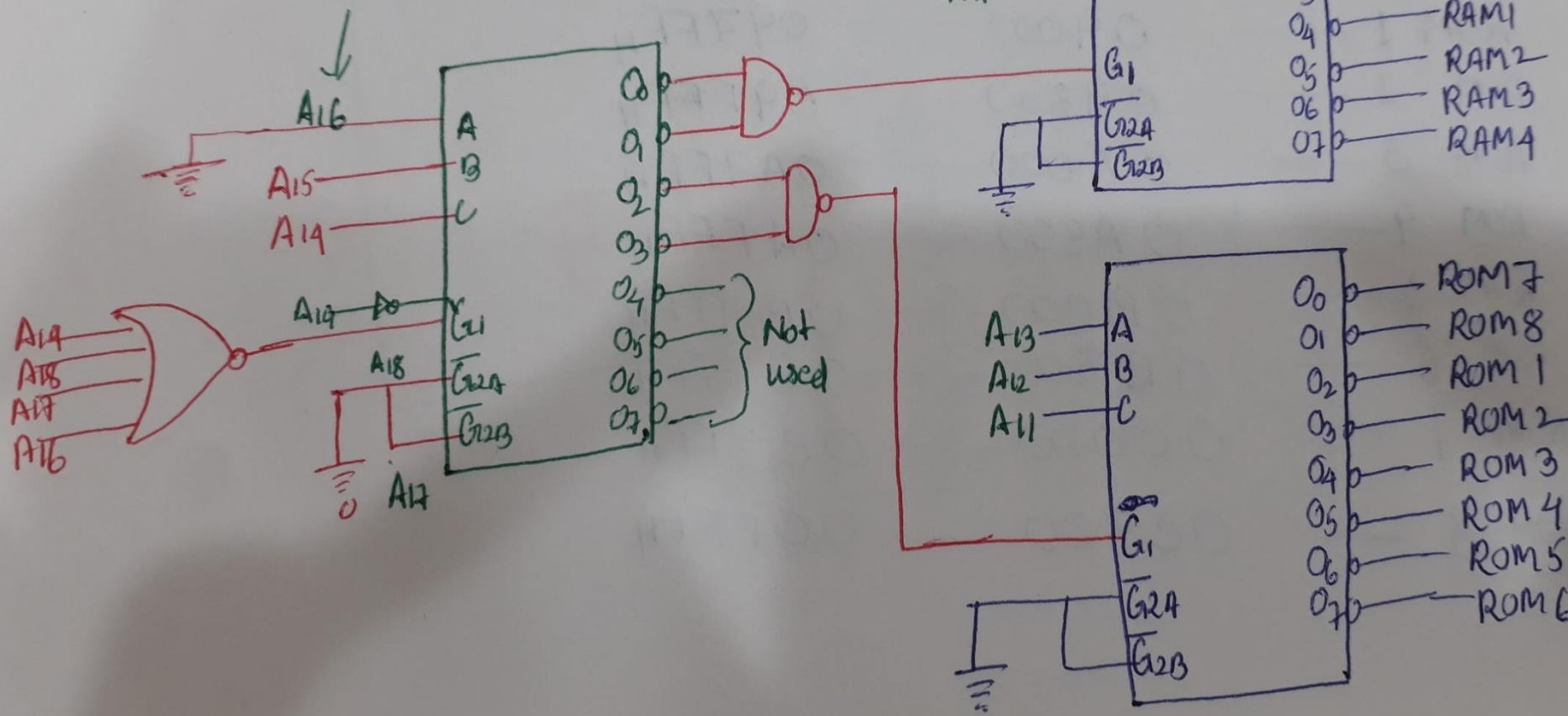
CHIP	A15	A14	A13	A12	A11	DECODE R O/P
RAM1	0	0	1	0	0	D1 O ₄
RAM2	0	0	1	0	1	D1 O ₅
RAM3	0	0	1	1	0	D1 O ₆
RAM4	0	0	1	1	1	D1 O ₇
RAM5	0	1	0	0	0	D1 O ₀
RAM6	0	1	0	0	1	D1 O ₁
RAM7	0	1	0	1	0	D1 O ₂
RAM8	0	1	0	1	1	D1 O ₃

Solution 2

CHIP	A15	A14	A13	A12	A11	DECODE R O/P
ROM1	1	0	0	1	0	D2 O ₂
ROM2	1	0	0	1	1	D2 O ₃
ROM3	1	0	1	0	0	D2 O ₄
ROM4	1	0	1	0	1	D2 O ₅
ROM5	1	0	1	1	0	D2 O ₆
ROM6	1	0	1	1	1	D2 O ₇
ROM7	1	1	0	0	0	D2 O ₀
ROM8	1	1	0	0	1	D2 O ₁

Solution 2

Green colour
↓ other option



Question 3

Design an 80286 based system that has the following memory requirements: (80286 – 24 Address Lines – 16 MB)

- 4M of ROM and the rest is RAM
- Half of the ROM - mapped to address space starting at 00 00 00_H
- Half to address space starting from E0 00 00_H
- The RAM is mapped continuously from address 20 00 00H.

Available Chips:

1M ROM -4

1M RAM -12

LS138-4

Solution 3

- Total memory =16 MB
- Given 4 MB ROM so 12 MB RAM
- 2MB - from 000000_H
- 2MB - from $E00000_H$
- 12MB - from 200000_H

Available Chips:

1MB ROM -4 chips --- A_0 - A_{10}

1MB RAM -12 chips--- A_0 - A_{10}

LS138 - 2

Solution 3

- ROM_{1E}---000000,000002,.....1FFFFE_H
- ROM₁₀---000001,000003,.....1FFFFFF_H
- ROM_{2E}--E00000,E00002,.....FFFFFFE_H
- ROM₂₀---E00001,E00003,.....FFFFFF_H
- RAM₁---- 200000—3FFFFFF_H
- RAM₂---- 400000—5FFFFFF_H
- RAM₃---- 600000—7FFFFFF_H
- RAM₄---- 800000—9FFFFFF_H
- RAM₅---- A00000—BFFFFFF_H
- RAM₆---- C00000—DFFFFFF_H

1K	10 Lines
2K	11 Lines
4K	12 Lines
8K	13 Lines
16 K	14 Lines
32 K	15 Lines
64 K	16 Lines
128 K	17 Lines
256 K	18 Lines
512 K	19 Lines
1M	20 Lines

1M	20 Lines	1111-1111-1111-1111-1111
2M	21 Lines	1FFFFFF

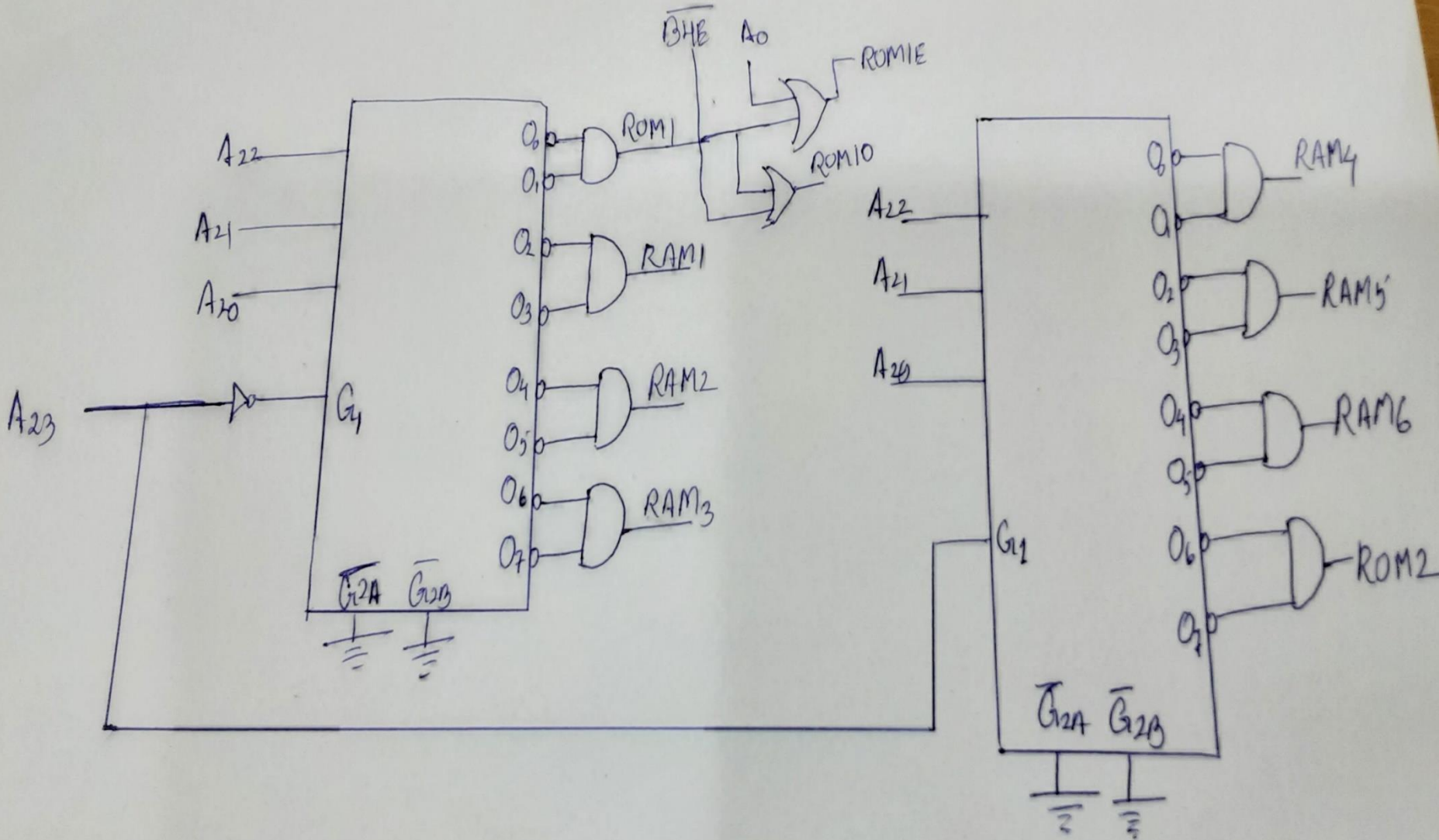
Solution 3

CHIP	A23	A22	A21	A20	DECODER O/P
ROM ₁	0	0	0	0	D1 O ₀
ROM ₁	0	0	0	1	D1 O ₁
ROM ₂	1	1	1	0	D2 O ₆
ROM ₂	1	1	1	1	D2 O ₇

Solution 3

CHIP	A23	A22	A21	A20	DECODER O/P
RAM1	0	0	1	0	D1 O ₂
RAM1	0	0	1	1	D1 O ₃
RAM2	0	1	0	0	D1 O ₄
RAM2	0	1	0	1	D1 O ₅
RAM3	0	1	1	0	D1 O ₆
RAM3	0	1	1	1	D1 O ₇
RAM4	1	0	0	0	D2 O ₀
RAM4	1	0	0	1	D2 O ₁
RAM5	1	0	1	0	D2 O ₂
RAM5	1	0	1	1	D2 O ₃
RAM6	1	1	0	0	D2 O ₄
RAM6	1	1	0	1	D2 O ₅

Solution 3





Thank You