

MPI Tutorial-10 8086 Memory Interface

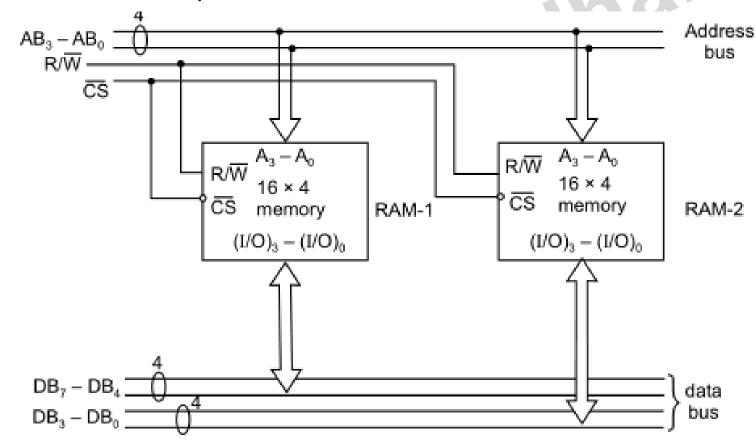
By Dr. Sanjay Vidhyadharan



Design a memory having size 16×8 from 16×4 memory modules. Draw the Schematic showing the Address Bus , Data Bus and Chip Select Lines Connection to the Chip.

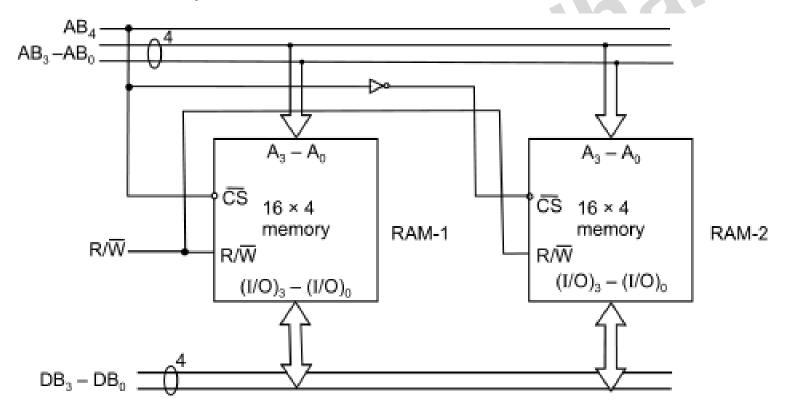
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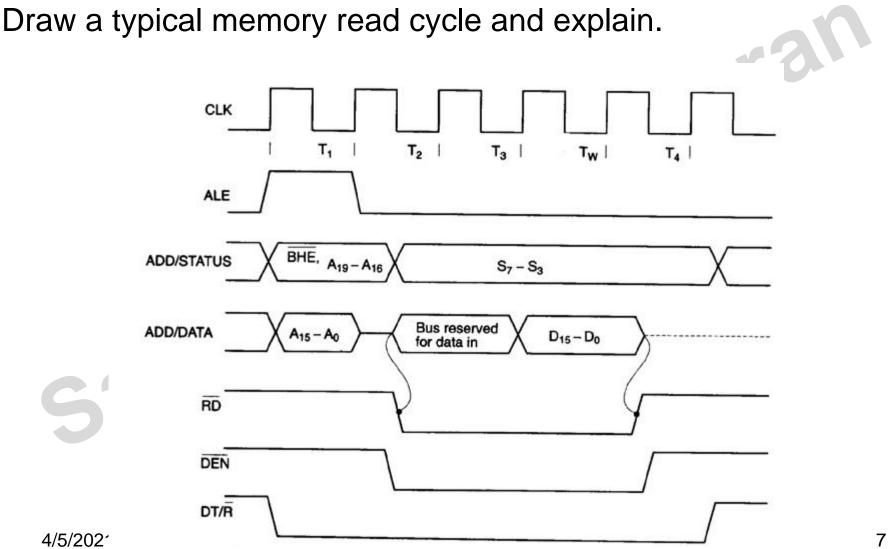


Develop a 32 × 4 memory module by combining two 16 × 4 memory chips. Draw the Schematic showing the Address Bus , Data Bus and Chip Select Lines Connection to the Chip.

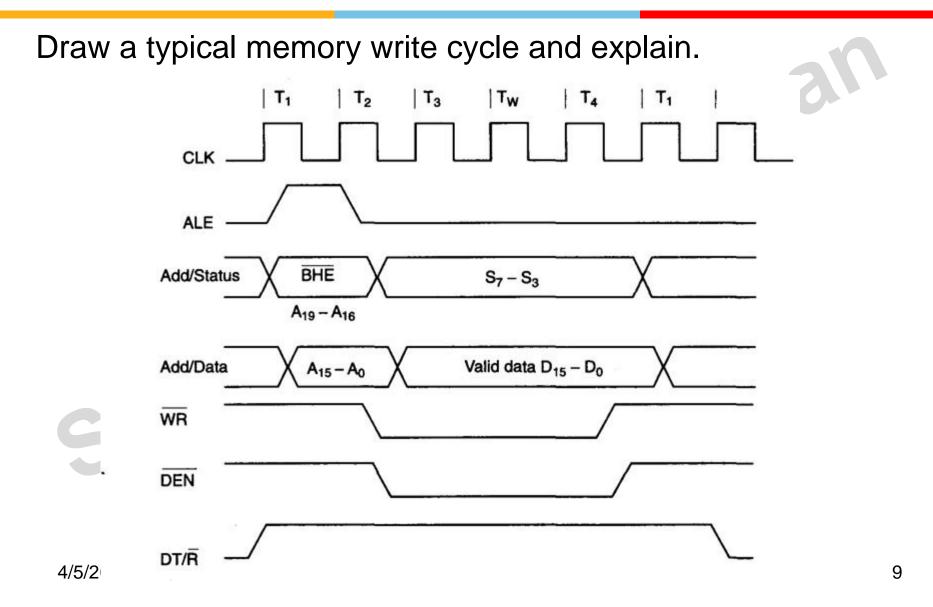
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Draw a typical memory read cycle and explain.



Draw a typical memory write cycle and explain.



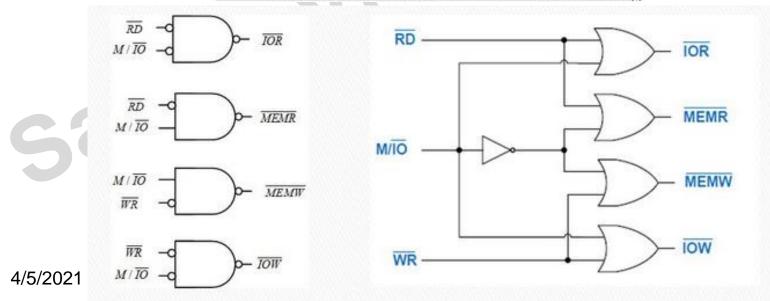
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Show how the MEMR and MEMW signals are derived from M/ IO', RD' and WR' signals of 8086.

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M/10	RD	WR	Operation
0	0	1	I/O read
Ó	1	0	I/O write
1	0	1	Memory read
1	1	0	Memory write



Design an interface between CPU 8086 and two chips of 32K X 8 ROM and four chips of 32 K X 8 RAM according to the following memory map

ROM 1 and ROM 2 \Rightarrow F0000H-FFFFFH RAM 1 and RAM 2 \Rightarrow D0000H-DFFFFH RAM 3 and RAM 4 \Rightarrow E0000H-EFFFFH

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Design an interface between CPU 8086 and two chips of 32K X 8 ROM and four chips of 32 K X 8 RAM according to the following memory map

ROM 1 and ROM 2 ⇒ F0000H–FFFFFH

RAM 1 and RAM 2 ⇒ D0000H–DFFFFH

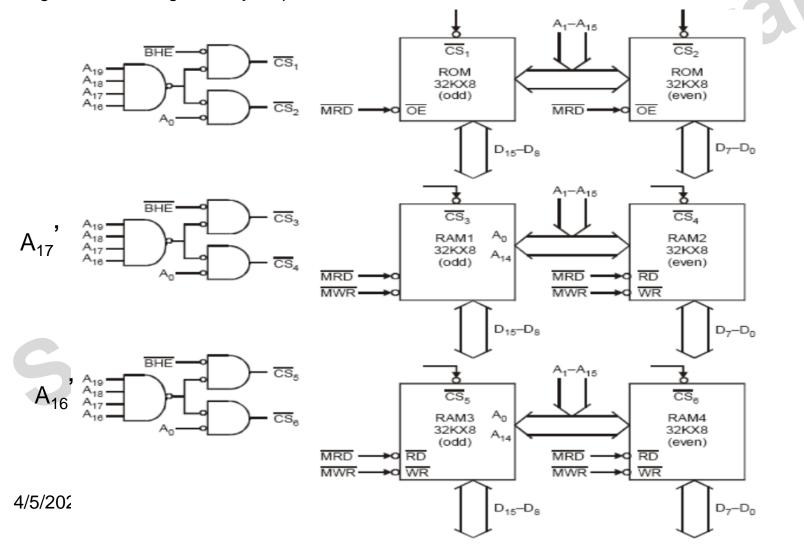
RAM 3 and RAM 4 ⇒ E0000H–EFFFFH

Solution.

Address Map

Address	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A ₀
FOOOOH ROM 1		1 ROM	1 2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FFFFFH	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
роооон	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RAM	1 and	RA	Л2																	
DFFFFH	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
EOOOOH	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RAM	3 and	4																		
EFFFFH	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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Thank You sanias