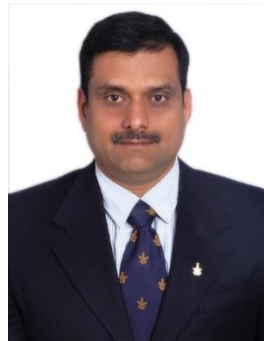




MPI Tutorial-10

8086 Memory Interface

By Dr. Sanjay Vidhyadharan



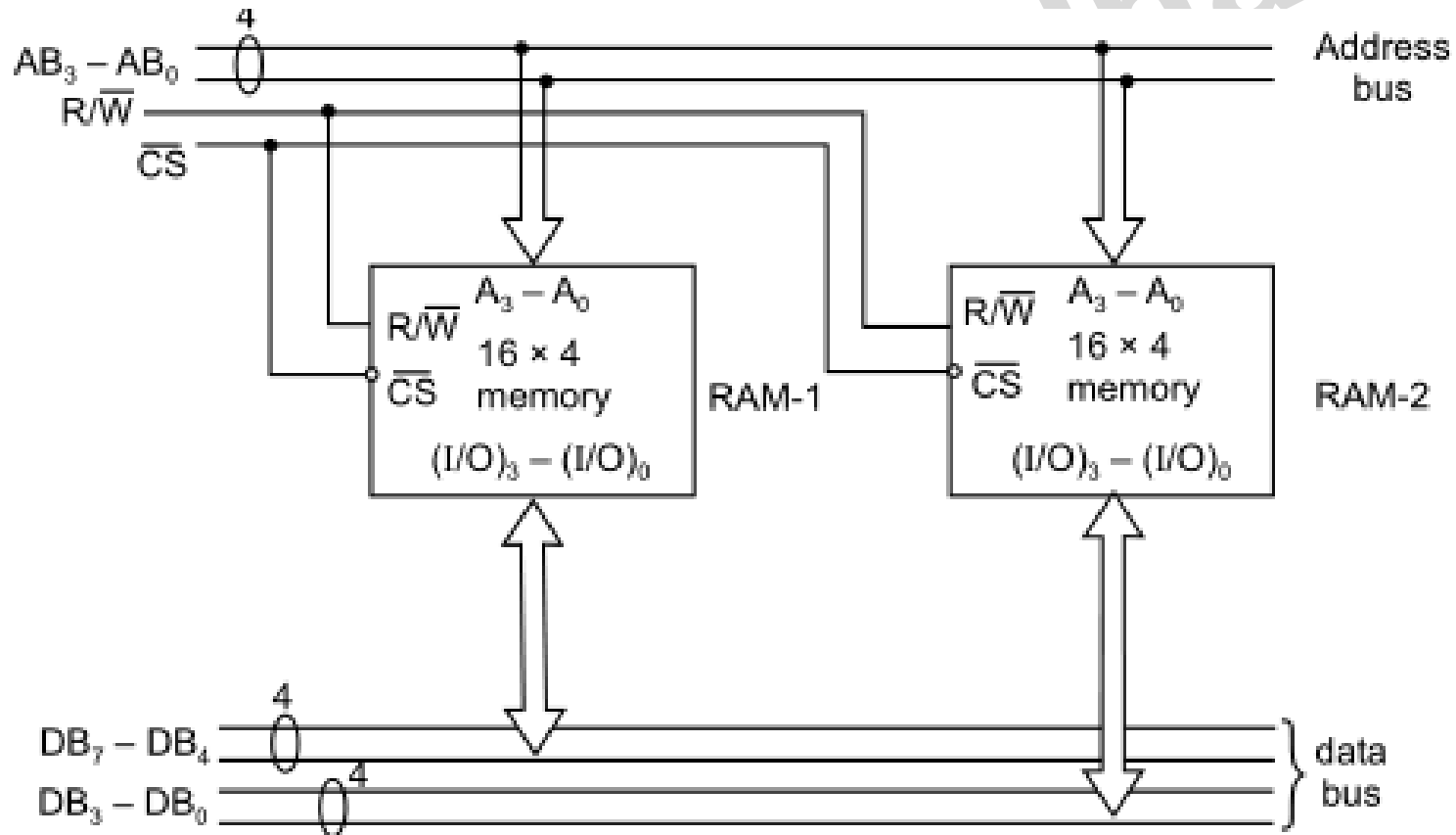
Problem-1

Design a memory having size 16×8 from 16×4 memory modules. Draw the Schematic showing the Address Bus , Data Bus and Chip Select Lines Connection to the Chip.

Sanjay Vidhyadharan

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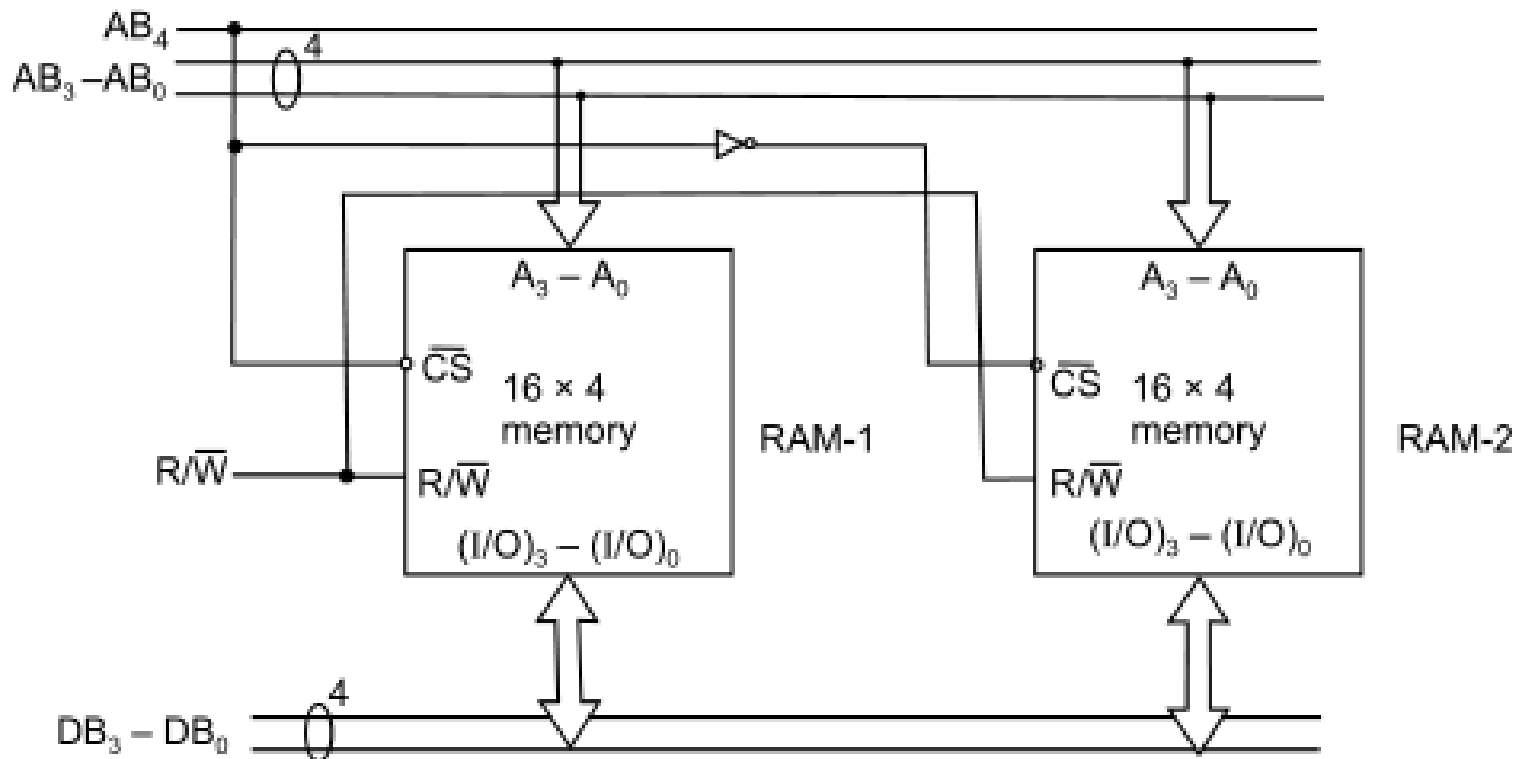


Problem-2

Develop a 32×4 memory module by combining two 16×4 memory chips. Draw the Schematic showing the Address Bus, Data Bus and Chip Select Lines Connection to the Chip.

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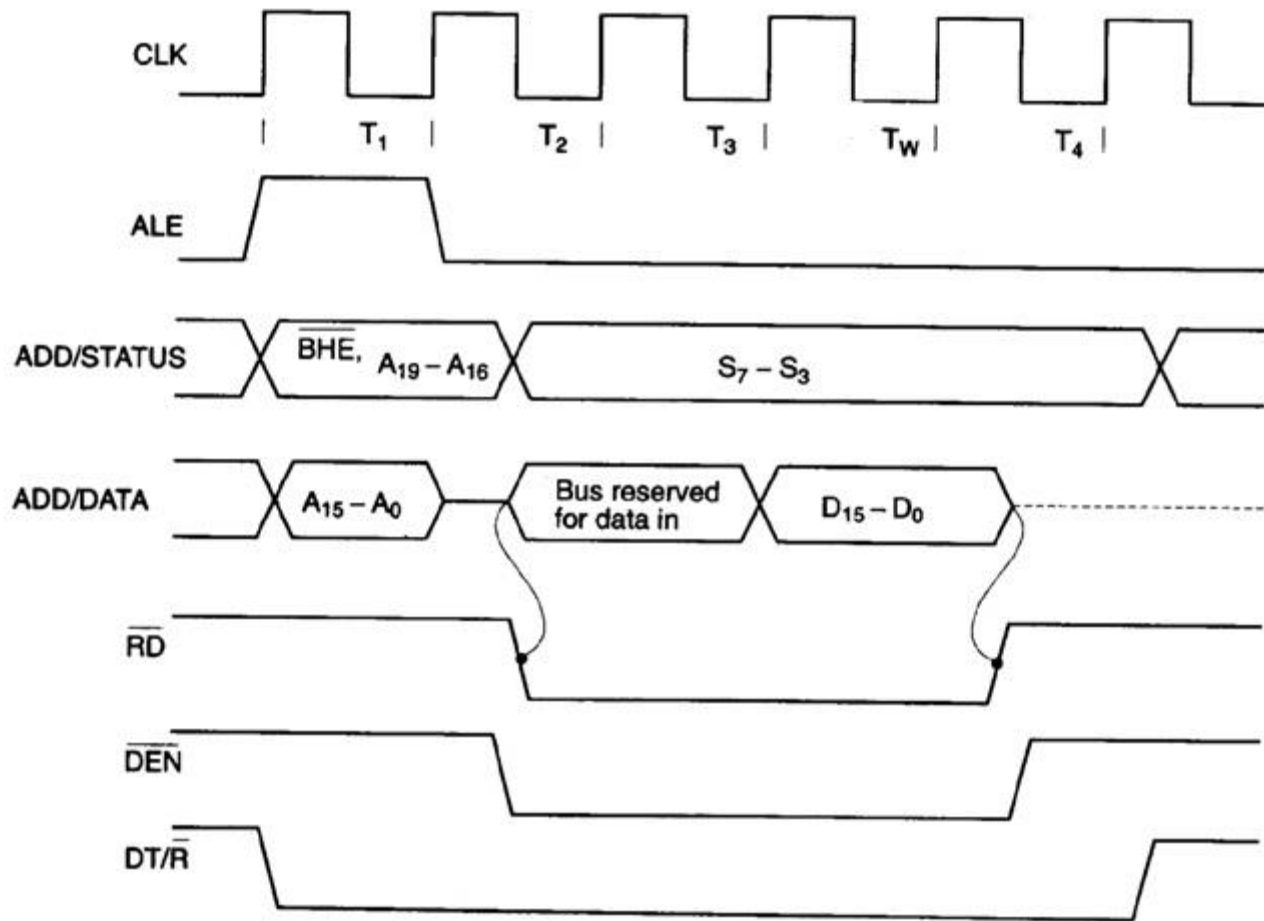
Problem-3

Draw a typical memory read cycle and explain.

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Problem-3

Draw a typical memory read cycle and explain.



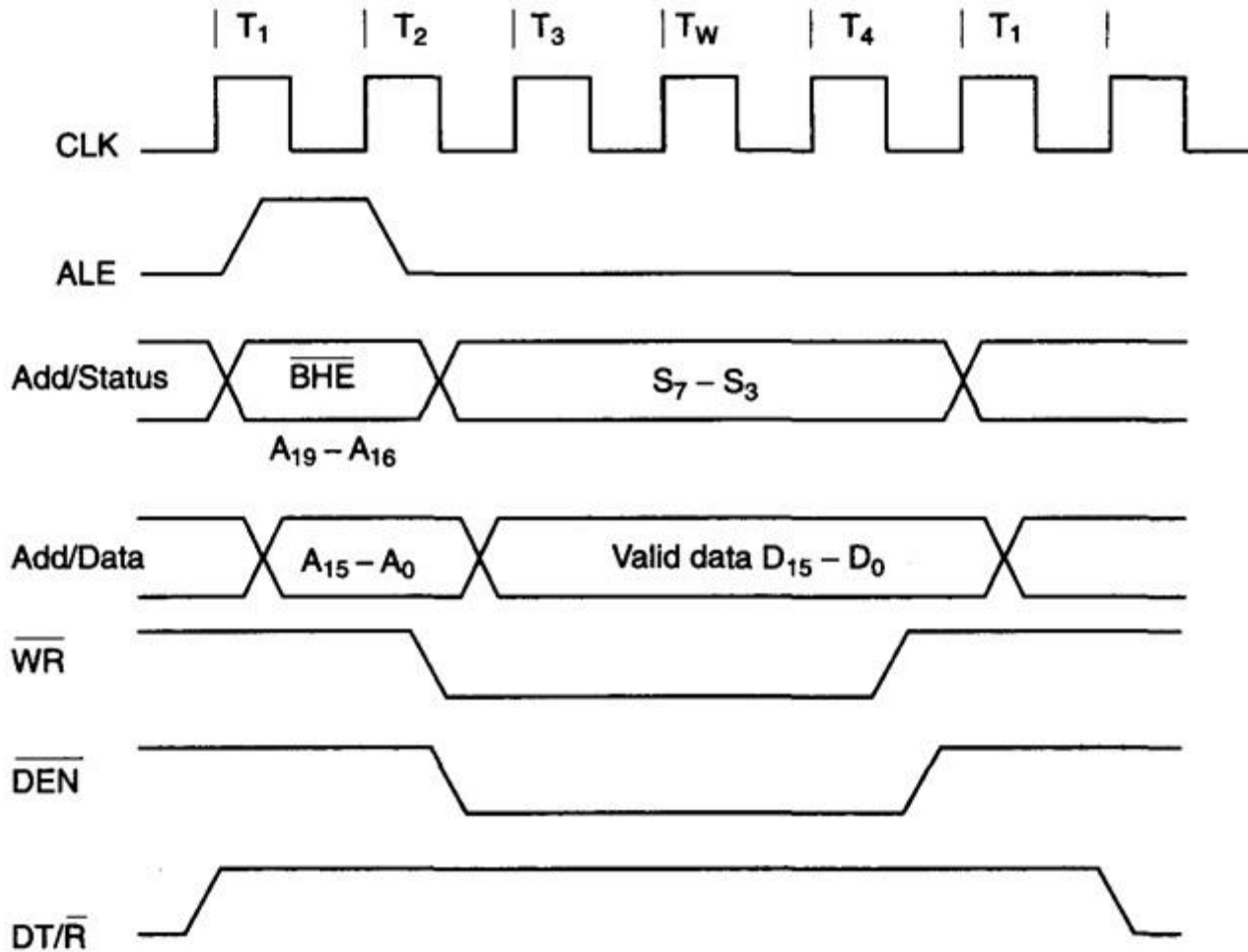
Problem-4

Draw a typical memory write cycle and explain.

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Problem-4

Draw a typical memory write cycle and explain.



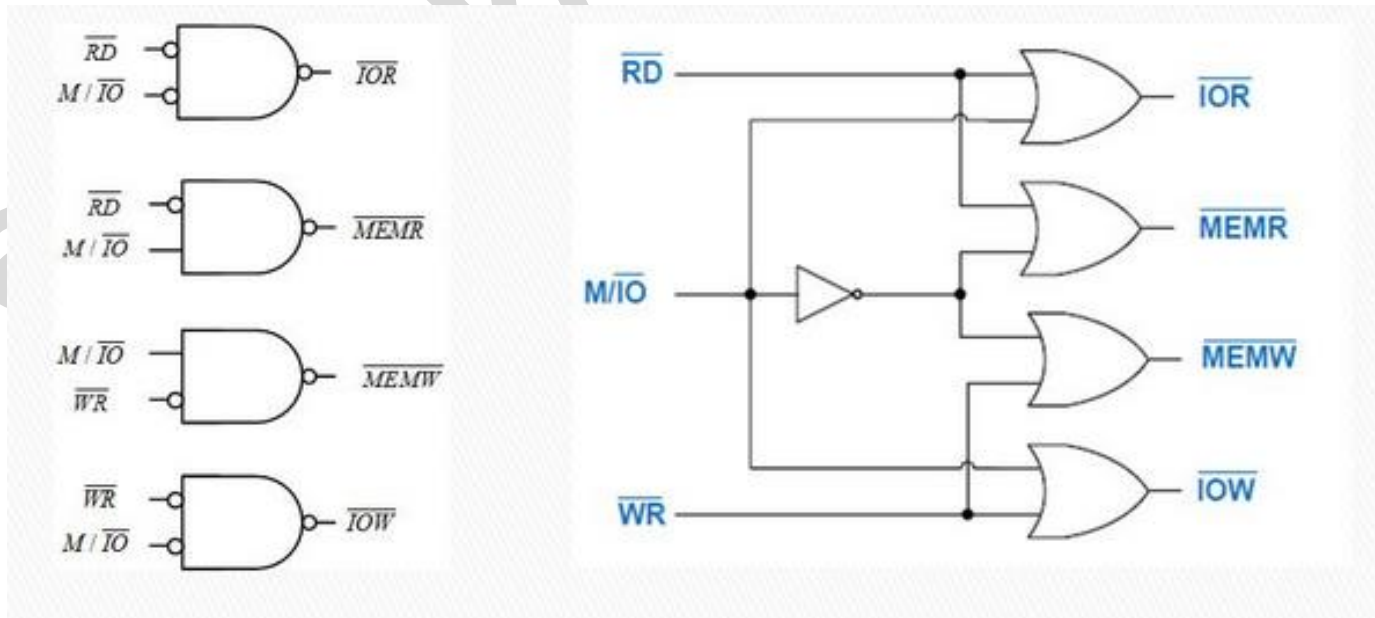
Problem-5

Show how the $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ signals are derived from $\text{M/ IO}'$, RD' and WR' signals of 8086.

Problem-5

Show how the \overline{MEMR} and \overline{MEMW} signals are derived from M/\overline{IO} , \overline{RD} and \overline{WR} signals of 8086.

M/\overline{IO}	\overline{RD}	\overline{WR}	Operation
0	0	1	I/O read
0	1	0	I/O write
1	0	1	Memory read
1	1	0	Memory write



Problem-6

Design an interface between CPU 8086 and two chips of 32K X 8 ROM and four chips of 32 K X 8 RAM according to the following memory map

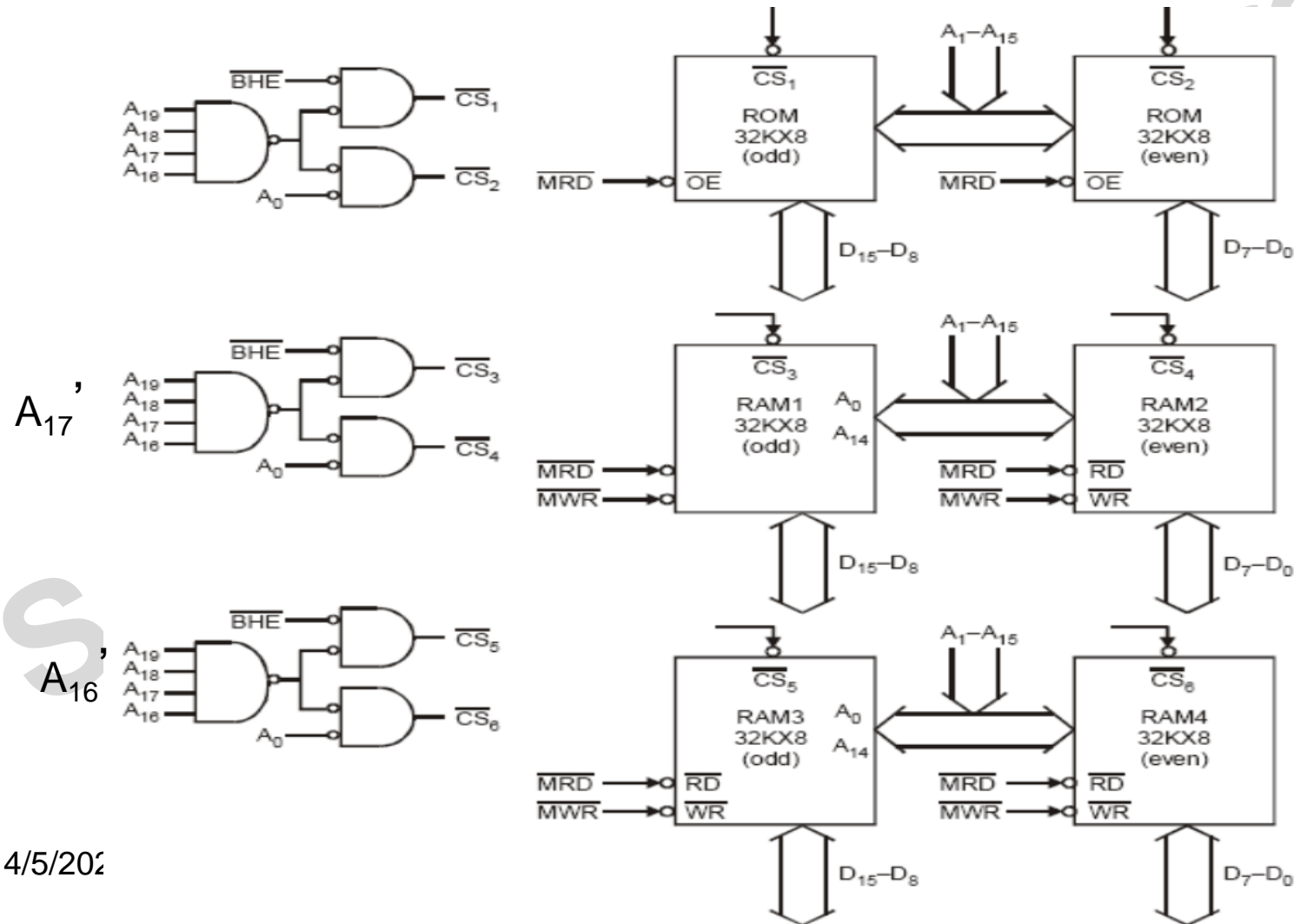
ROM 1 and ROM 2 \Rightarrow F0000H–FFFFFH

RAM 1 and RAM 2 \Rightarrow D0000H–DFFFFH

RAM 3 and RAM 4 \Rightarrow E0000H–EFFFFH

Problem-6

Design an interface between CPU 8086 and two chips of 32K X 8 ROM and four chips of 32 K X 8 RAM according to the following memory map





Thank You