

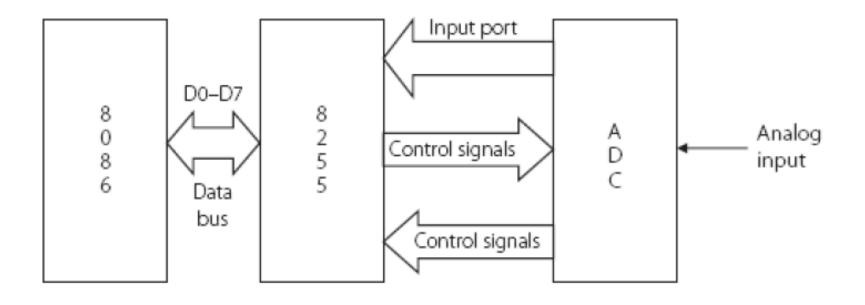
Microprocessors and Interfaces: 2021-22 Lecture 32

ANALOG-TO-DIGITAL (ADC) & DIGITAL-TO-ANALOG (DAC) CONVERTERS By Dr. Sanjay Vidhyadharan



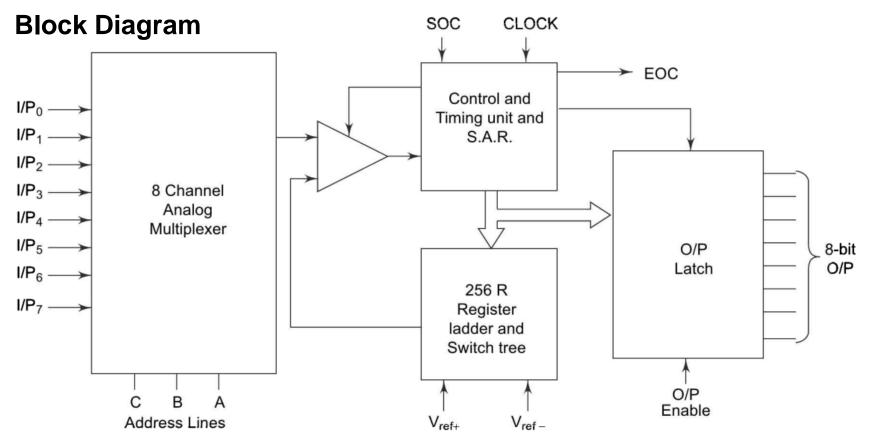
ADC (Analog-to Digital Converter)

Interface with 8086



SOC: Start of Conversion EOC : End of Conversion

531



Low-cost ADC, Power 15 mW,

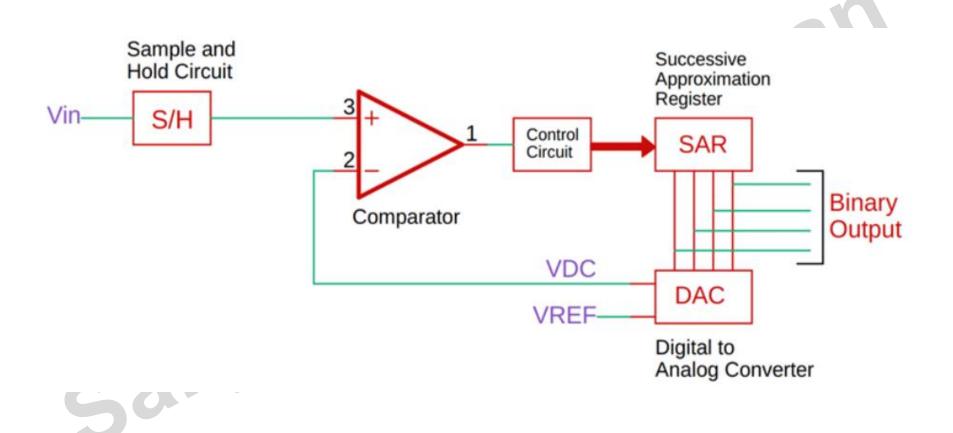
Compatible with a wide range of microprocessors. Power Supply 5 V Moderate speed 100 μ s Moderate accuracy Error <u>+</u> LSB ₃

Pin Diagram

				1					
$I/P_3 \rightarrow$	1		28	-	I/P2				
$I/P_4 \rightarrow$	2		27	← I/P1	I/P1				
$I/P_5 \rightarrow$	3		26	-	← I/Po	I/P ₀ –I/P ₇	Analog inputs Address lines for s		
$I/P_6 \rightarrow$	4		25	-	ADD A	ADD A, B, C			
$I/P_7 \rightarrow$	5		24	-	ADD B	O ₇ –O ₀	Digital 8-bit outpu		
SOC→	6		23	-	ADD C	SOC	Start of conversion		
EOC→	7	ADC 0808	22	-	ALE	EOC	End of conversion		
$O_3 \rightarrow$	8	ADC 0809	21	-	O7MSB	OE	Output latch enab		
OE →	9		20	-	O ₆	CLK	Clock input for AD		
CLK ->	10		19	-	O ₅	V _{CC} , GND	Supply pins +5V a		
$V_{CC} \rightarrow$	11		18	-	O ₄	V_{ref+} and V_{ref-}	Reference voltage		
$V_{ref^+} \rightarrow$	12		17	-	O ₀ LSB		and Reference vo		
GND→	13		16	-	V _{ref} -				
0 ₁ →	14		15	-	O ₂				
]					
	$I/P_{4} \rightarrow I/P_{5} \rightarrow I/P_{6} \rightarrow I/P_{7} \rightarrow SOC \rightarrow EOC \rightarrow O_{3} \rightarrow OE \rightarrow CLK \rightarrow V_{CC} \rightarrow V_{ref^{+}} \rightarrow V_{r$	$I/P_{4} \rightarrow 2$ $I/P_{5} \rightarrow 3$ $I/P_{6} \rightarrow 4$ $I/P_{7} \rightarrow 5$ $SOC \rightarrow 6$ $EOC \rightarrow 7$ $O_{3} \rightarrow 8$ $OE \rightarrow 9$ $CLK \rightarrow 10$ $V_{cc} \rightarrow 11$ $V_{ref^{+}} \rightarrow 12$ $GND \rightarrow 13$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$I/P_4 \rightarrow 2$ 27 $I/P_5 \rightarrow 3$ 26 $I/P_6 \rightarrow 4$ 25 $I/P_7 \rightarrow 5$ 24 SOC \rightarrow 6 23 EOC \rightarrow 7 ADC 0808 22 $O_3 \rightarrow 8$ ADC 0809 21 OE \rightarrow 9 20 20 CLK \rightarrow 10 19 19 $V_{cc} \rightarrow 11$ 18 $V_{ref^+} \rightarrow 12$ 17 GND \rightarrow 13 16 20	$I/P_4 \rightarrow 2$ 27 $I/P_5 \rightarrow 3$ 26 $I/P_6 \rightarrow 4$ 25 $I/P_7 \rightarrow 5$ 24 SOC \rightarrow 6 23 $O_3 \rightarrow 8$ ADC 0808 21 $OE \rightarrow 9$ 20 $CLK \rightarrow 10$ 19 $V_{ref^+} \rightarrow 12$ 17 $GND \rightarrow 13$ 16	$I/P_4 \rightarrow 2$ $27 \leftarrow I/P1$ $I/P_5 \rightarrow 3$ $26 \leftarrow I/P0$ $I/P_6 \rightarrow 4$ $25 \leftarrow ADD A$ $I/P_7 \rightarrow 5$ $24 \leftarrow ADD B$ $SOC \rightarrow 6$ $23 \leftarrow ADD C$ $EOC \rightarrow 7$ $ADC \ 0808$ $21 \leftarrow O_7 MSB$ $O_3 \rightarrow 8$ $ADC \ 0809$ $21 \leftarrow O_7 MSB$ $OE \rightarrow 9$ $20 \leftarrow O_6$ $CLK \rightarrow 10$ $19 \leftarrow O_5$ $V_{cc} \rightarrow 11$ $18 \leftarrow O_4$ $V_{ref^+} \rightarrow 12$ $17 \leftarrow O_0 \ LSB$ $GND \rightarrow 13$ $16 \leftarrow V_{ref^-}$	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		

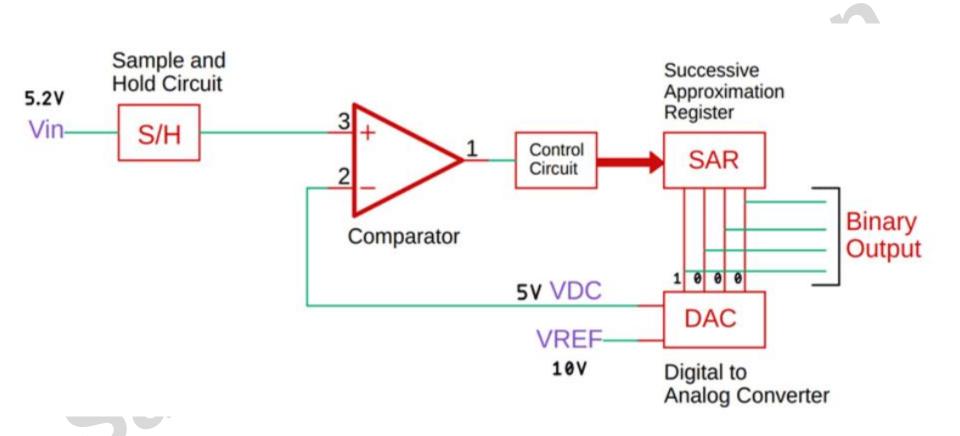
	Analog inputs
	Address lines for selecting analog inputs
	Digital 8-bit output with O ₇ MSB and O ₀ LSB
	Start of conversion signal pin
	End of conversion signal pin
	Output latch enable pin, if high enable output
	Clock input for ADC
	Supply pins +5V and GND
-	Reference voltage positive (+5 Volts maximum) and Reference voltage negative (0V minimum)

Successive Approximation ADC



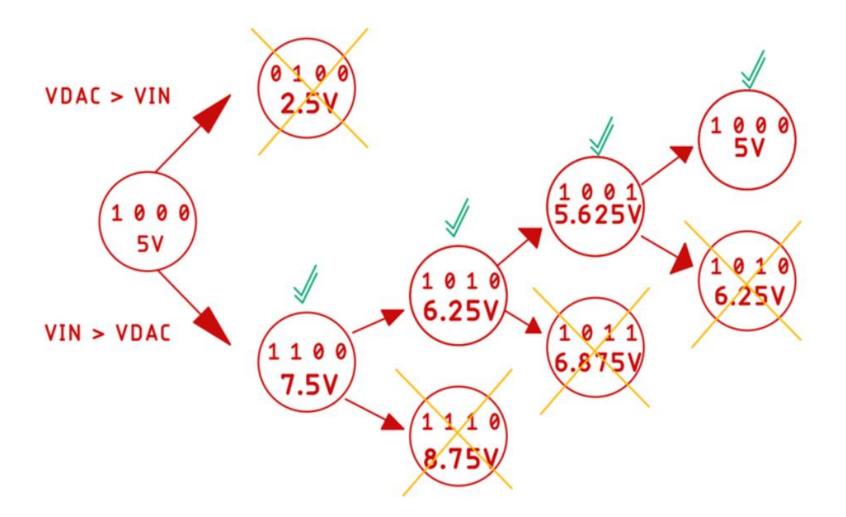


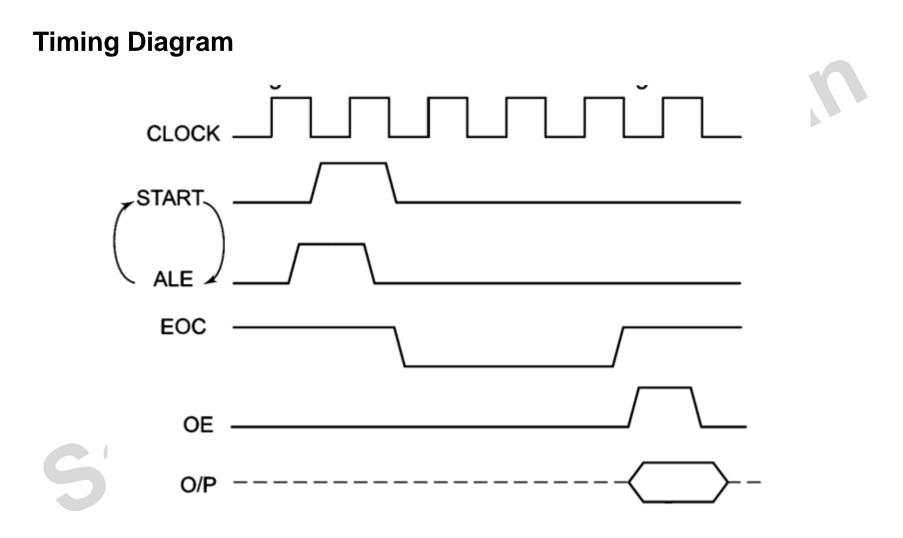
Successive Approximation ADC



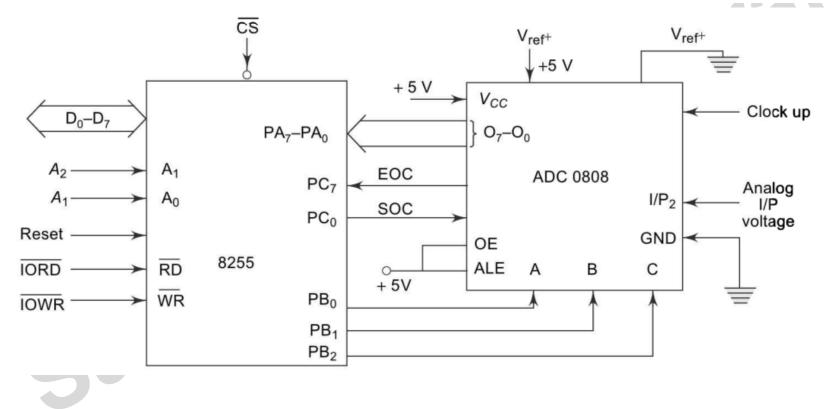


Successive Approximation ADC





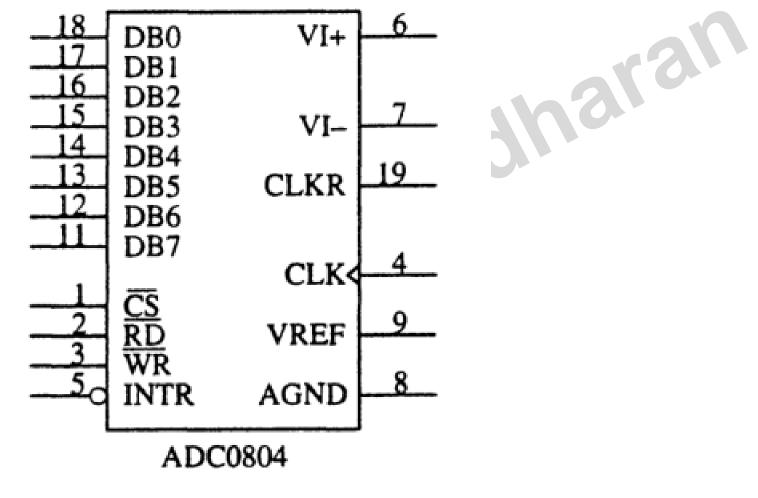
Interface ADC 0808 with 8086 using 8255 ports. Use Port A of 8255 for transferring digital data output of ADC to the CPU and Port C for control signals. Assume that an analog input is present at I/P_2 of the ADC and a clock input of suitable frequency is available for ADC. Draw the schematic and write required ALP.



Interface ADC 0808 with 8086 using 8255 ports. Use Port A of 8255 for transferring digital data output of ADC to the CPU and Port C for control signals. Assume that an analog input is present at I/P_2 of the ADC and a clock input of suitable frequency is available for ADC. Draw the schematic and write required ALP.

	D ₇	D ₆	D_5	D ₄	D3	D_2	D ₁		Do	Control w	vord
	1	0	0	1	1	0	0		0	= 98 H	D7=1; I/O Mode.
The required ALP is given as follows:											D6=0 and D5=0; Port A Mode
WAIT	·	OUT C MOV A OUT P MOV A OUT P MOV A OUT P IN AL RCL JNC W	L,O2H ORT B,A L,OOH ORT C,A L,O1 H ORT C,A L,OOH ORT C,A ,PORTC			• 7 • 7 • 7 • 7 • 7 • 7 • 7 • 7	pulse t Check f reading rotatin	ed a I/P ₂ art o th or E por g th	as an of co ne ADC C by t C u nrough	nalog nversior pper and carry.	D4=1; Port A is input port D3=1; Port C (Upper) is input D2=0; Port B Mode 0. D1=0; Port B is output D0=0; Port C (Lower) is output
		HLT				;	Stop				10

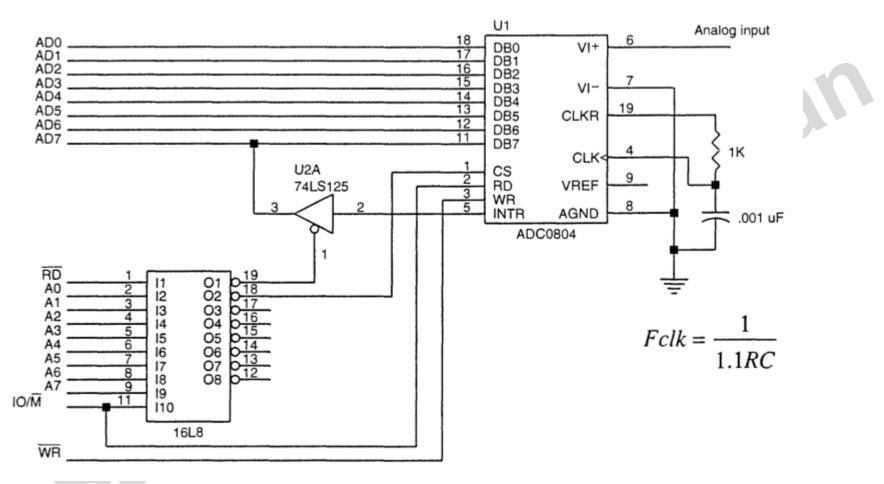




SOC: Start of Conversion WR' and CS' EOC : End of Conversion INTR

4/27/2021

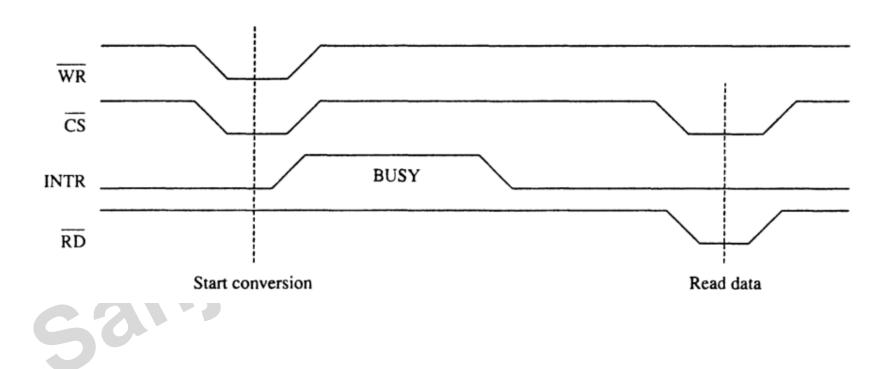
ADC 0804



Permissible range of clock frequencies is 100 KHz - 1460 KHz. desirable to use a frequency as close as possible to 1460 KHz so conversion time is minimized



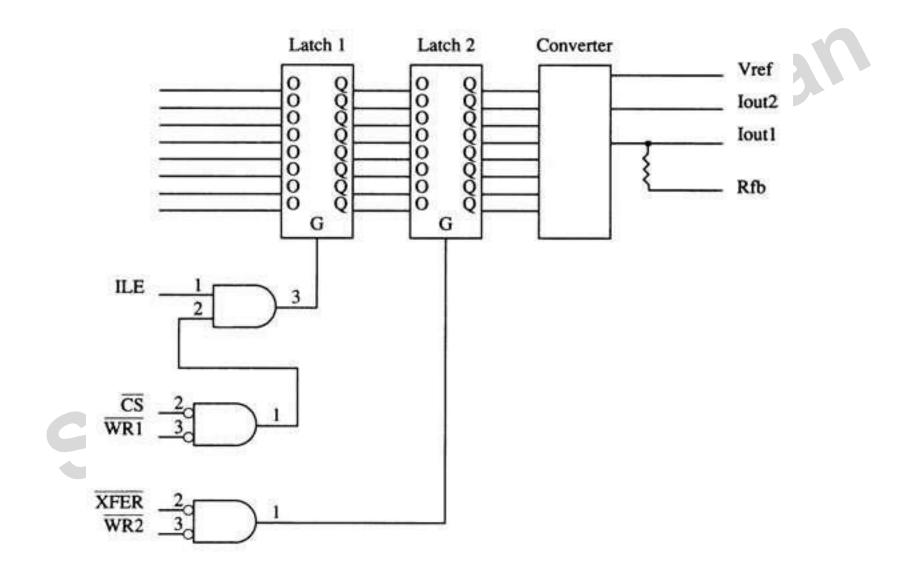




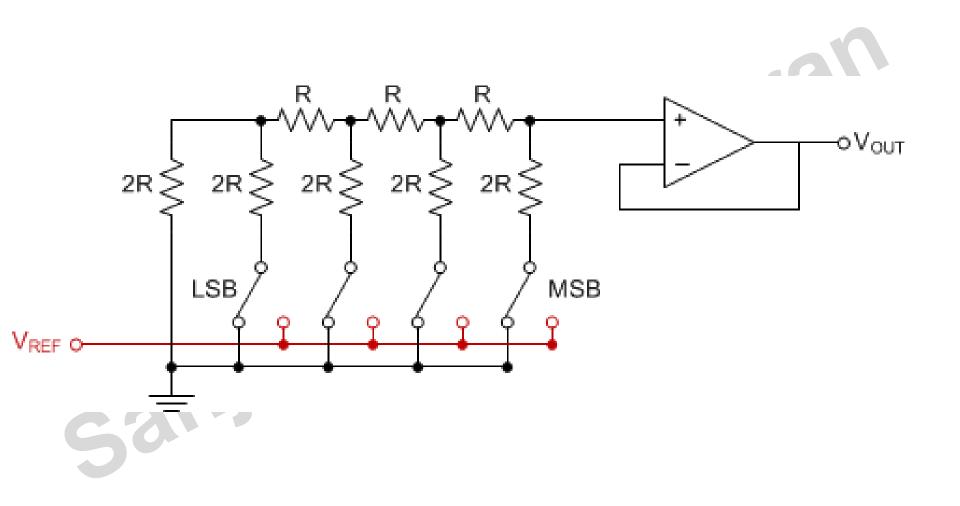


- A fairly common and low-cost digital-to-analog converter is the DAC0830.
- An 8-bit converter that transforms an 8-bit binary number into an analog voltage.
- Other converters are available that convert from 10-, 12-, or 16-bit binary numbers into analog voltages.

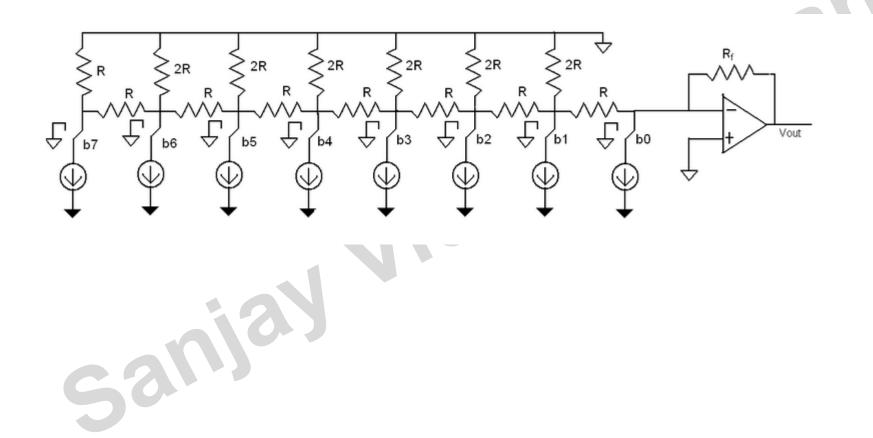
- The number of voltage steps generated by the converter is equal to the number of binary input combinations.
 - an 8-bit converter generates 256 voltage levels
 - a 10-bit converter generates 1024 levels
- The DAC0830 is a medium-speed converter that transforms a digital input to an analog output in approximately $1.0 \,\mu$ s.

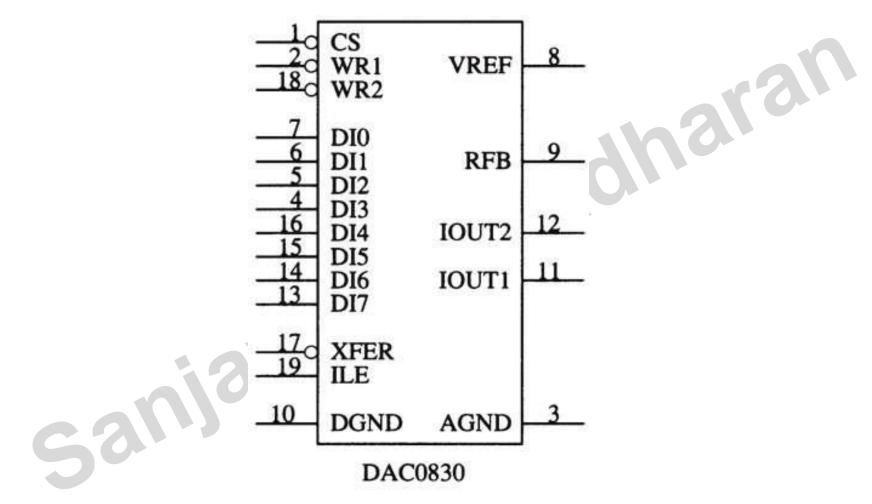


R-2R Ladder DAC

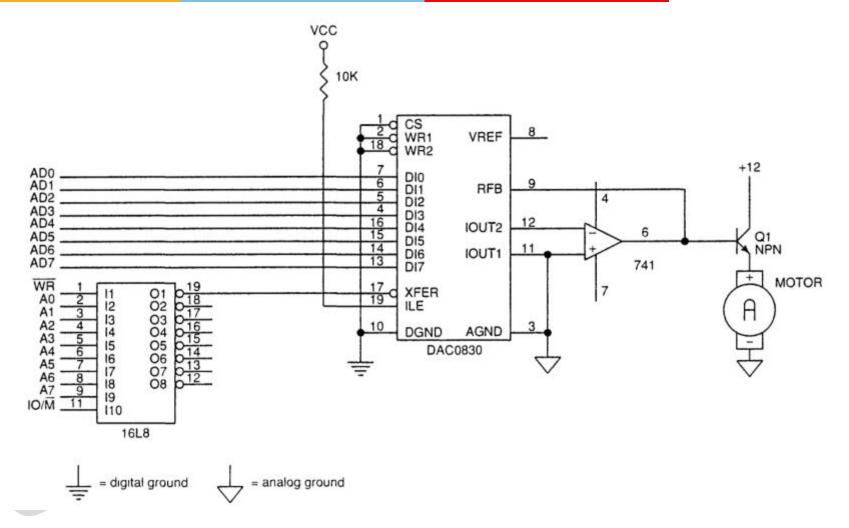


R-2R Ladder DAC





Because this is an 8-bit converter, its output step voltage is defined as $-V_{REF}$ (reference voltage), divided by 255. The step voltage is often called the resolution of the converter



Analog outputs labeled IOUT1 & IOUT2 are inputs to an external operational amplifier.

Thankyou

sanjay