Microprocessors and Interfaces: 2021-22
Lecture 30 :
8253/8254 Timer
Part:2

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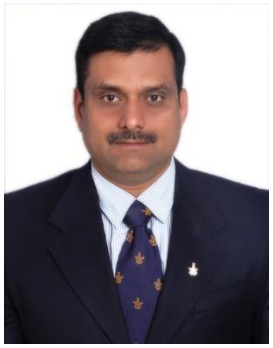
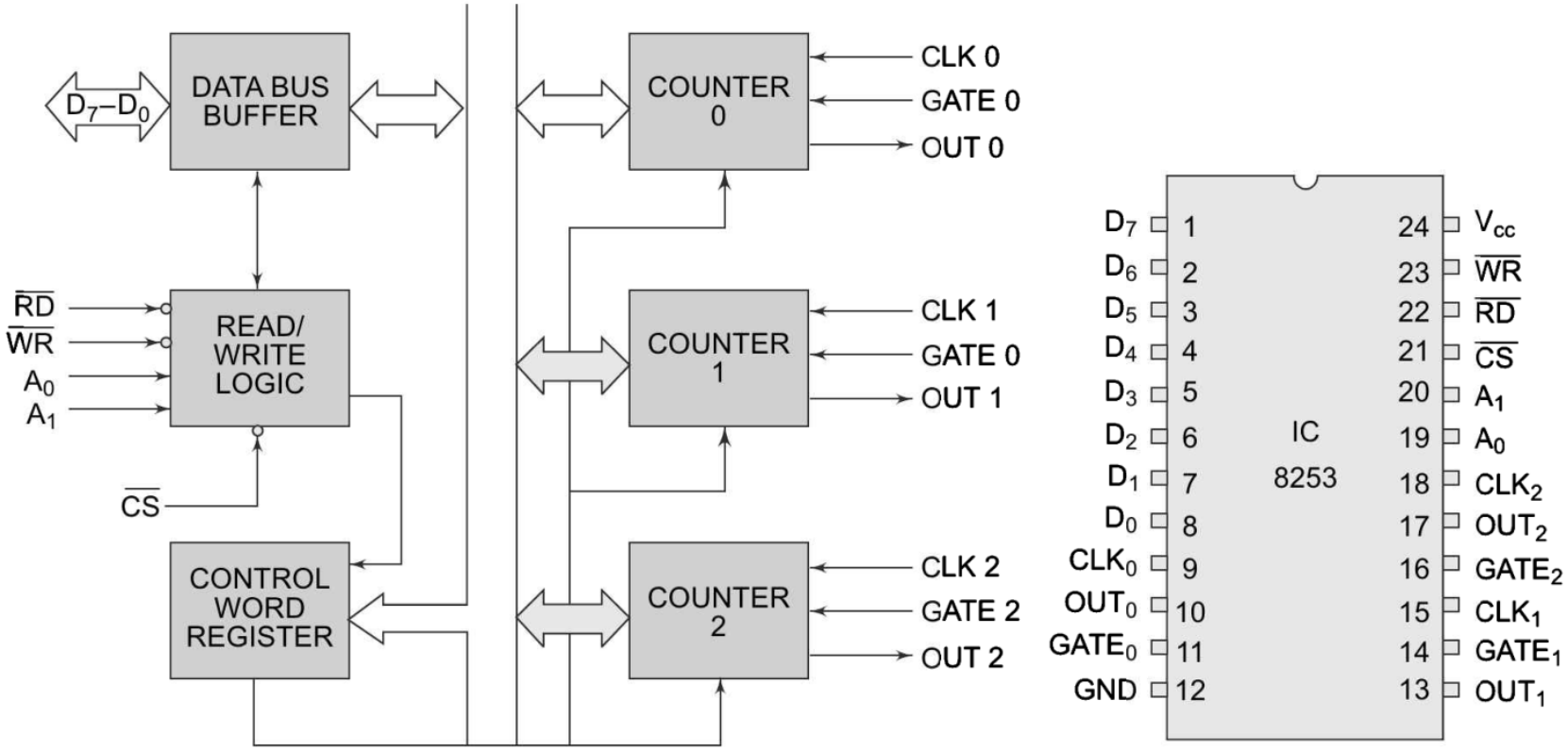


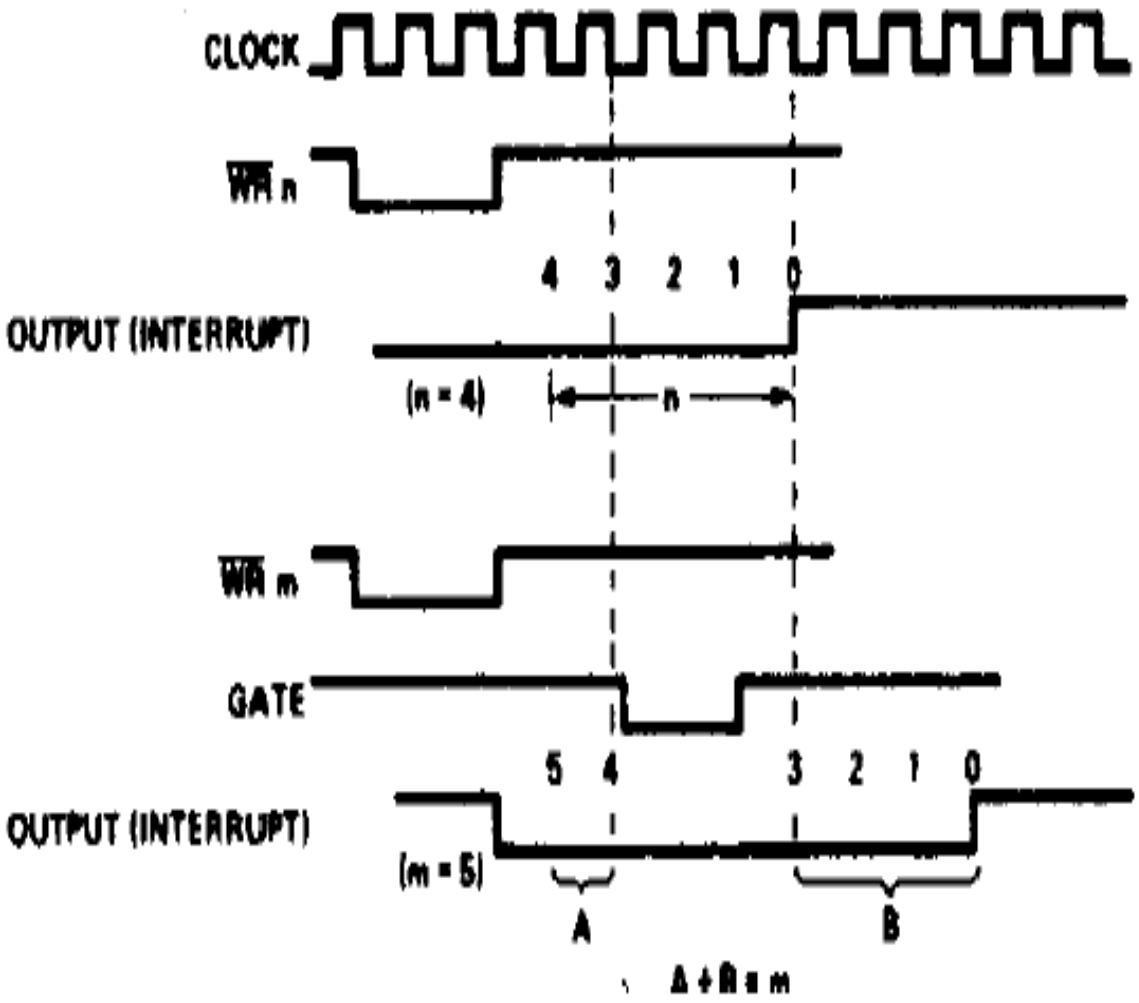
Pin diagram of 8253/8254



Mode 0 –Interrupt on Terminal count

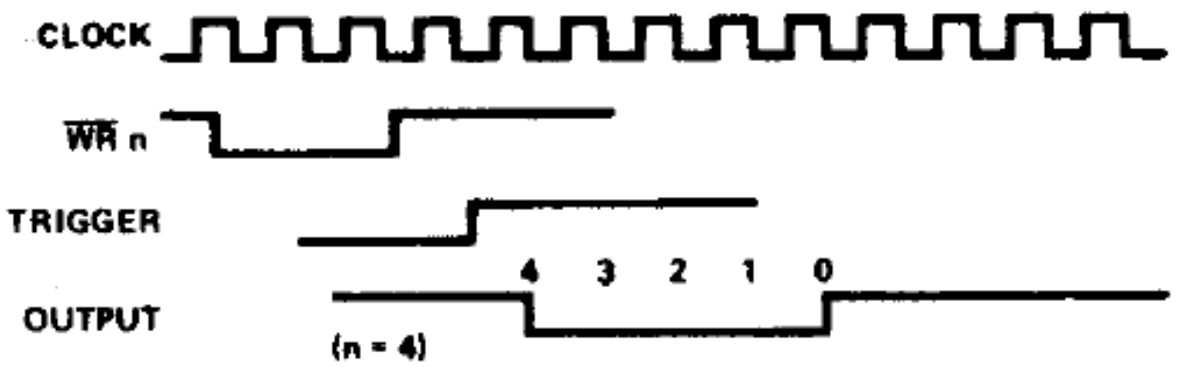
- Output goes high when TC is reached.
- Remains high till counter is re-loaded
- Writing first byte stops counting.
- Writing second byte starts new count.

use:
1. Self generated interrupt.
2. Programmable delayed event.

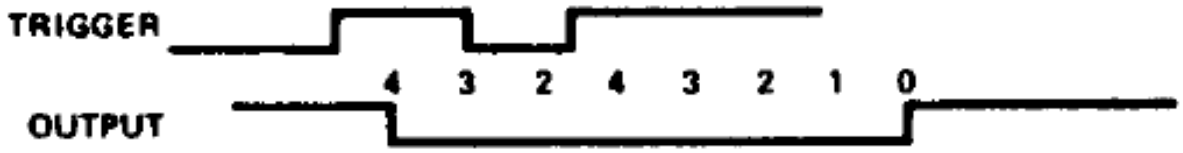


Mode 1 –Hardware retriggerable one-shot

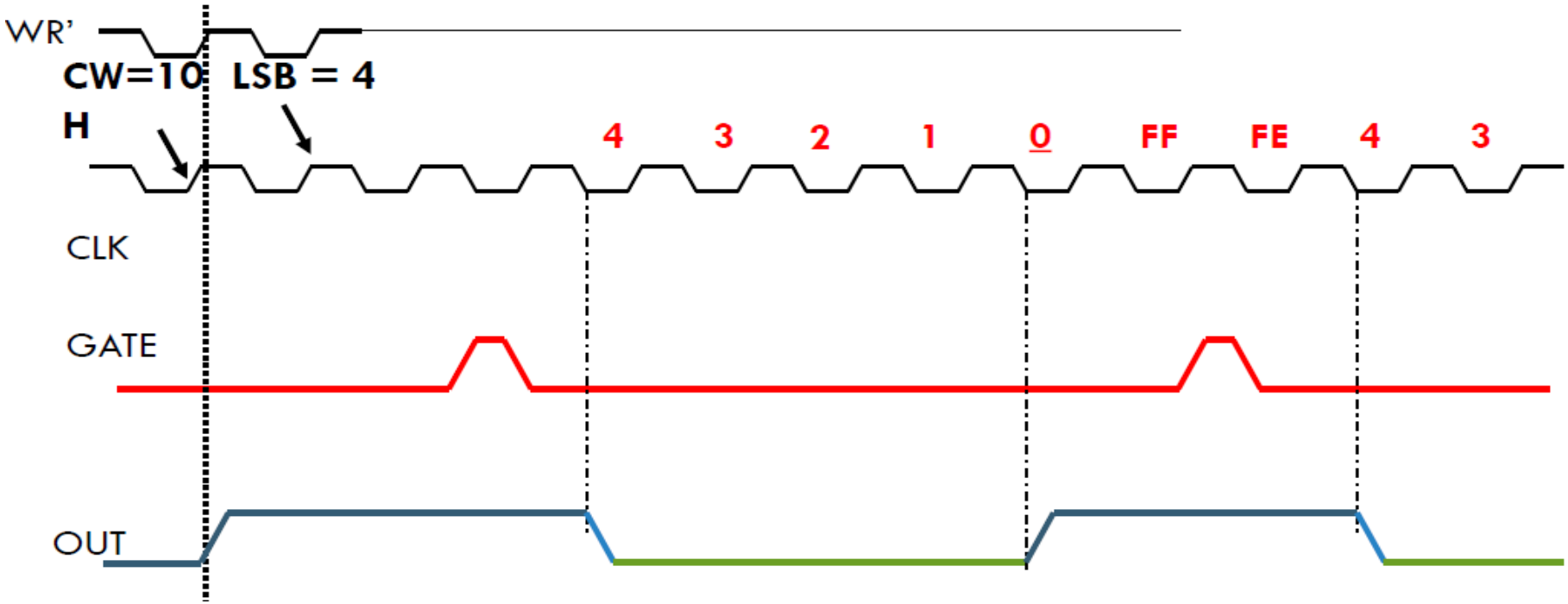
1. Output goes low following raising edge on gate
2. Output goes high when TC is reached.
3. Current output not effected by reloading count.
4. Re-triggerable



Use:
1. To create a time window for valid operations
2. Programmable pulse width.
3. To measure no activity (silence) for the given period.

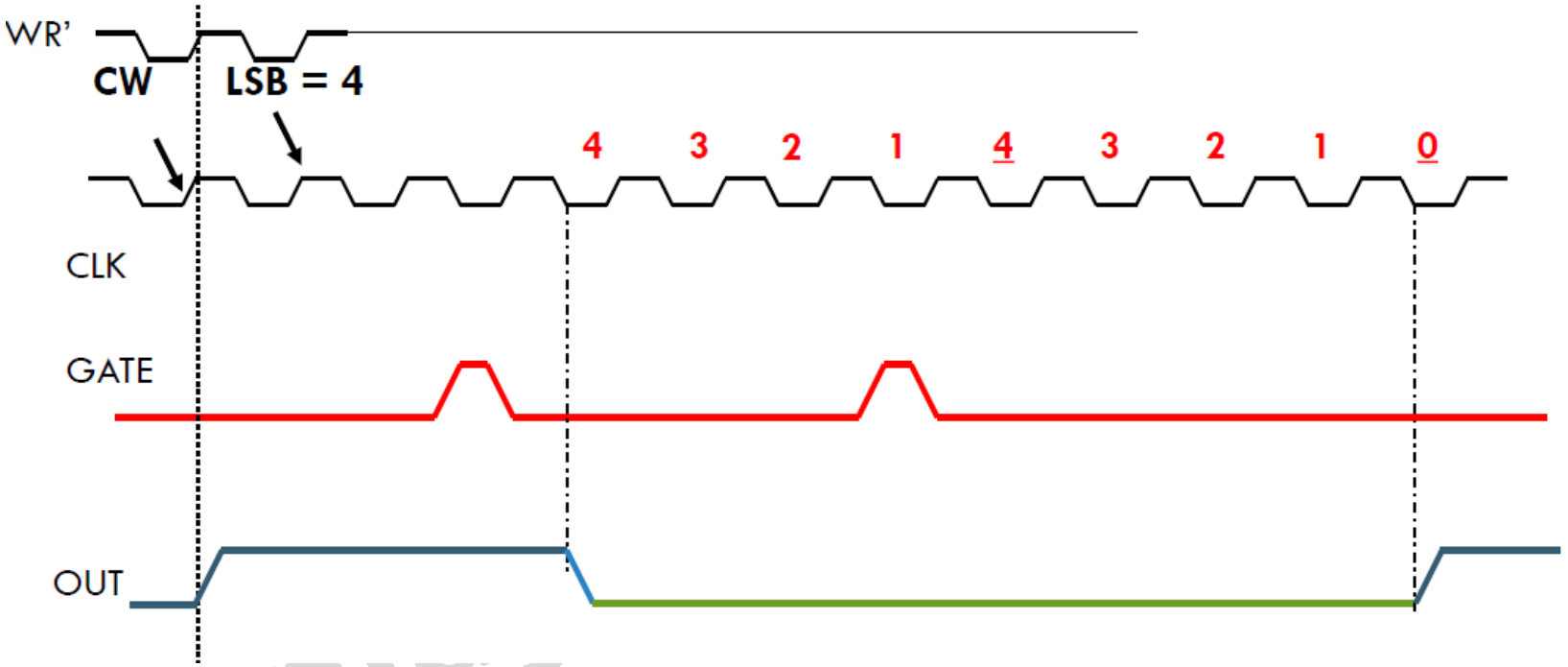


Mod 1: Case 1



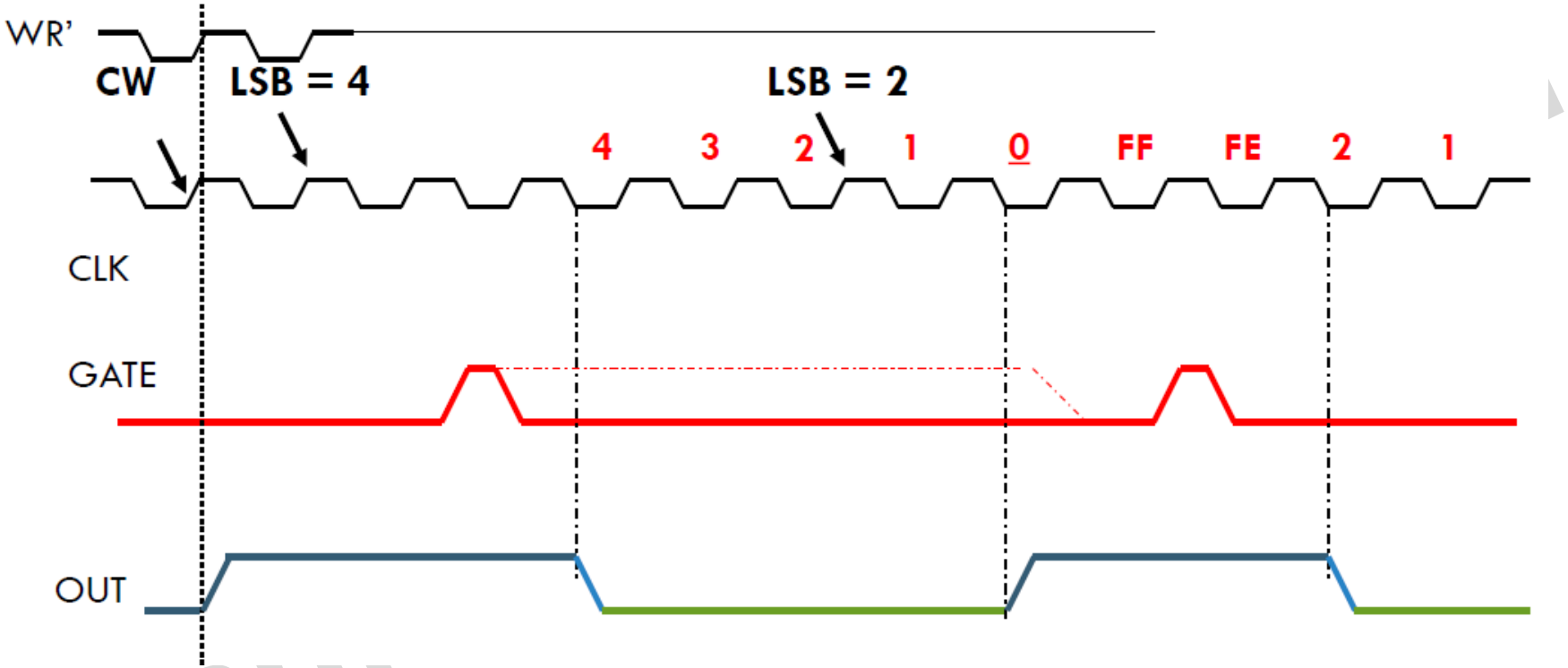
- Two step process
  - Load count register
  - Send 0-to-1 pulse on GATE to trigger it
- When triggered ⇒ o/p goes low after one clock cycle & stays low for N clock cycles ⇒ goes high

Mod 1: Case 2



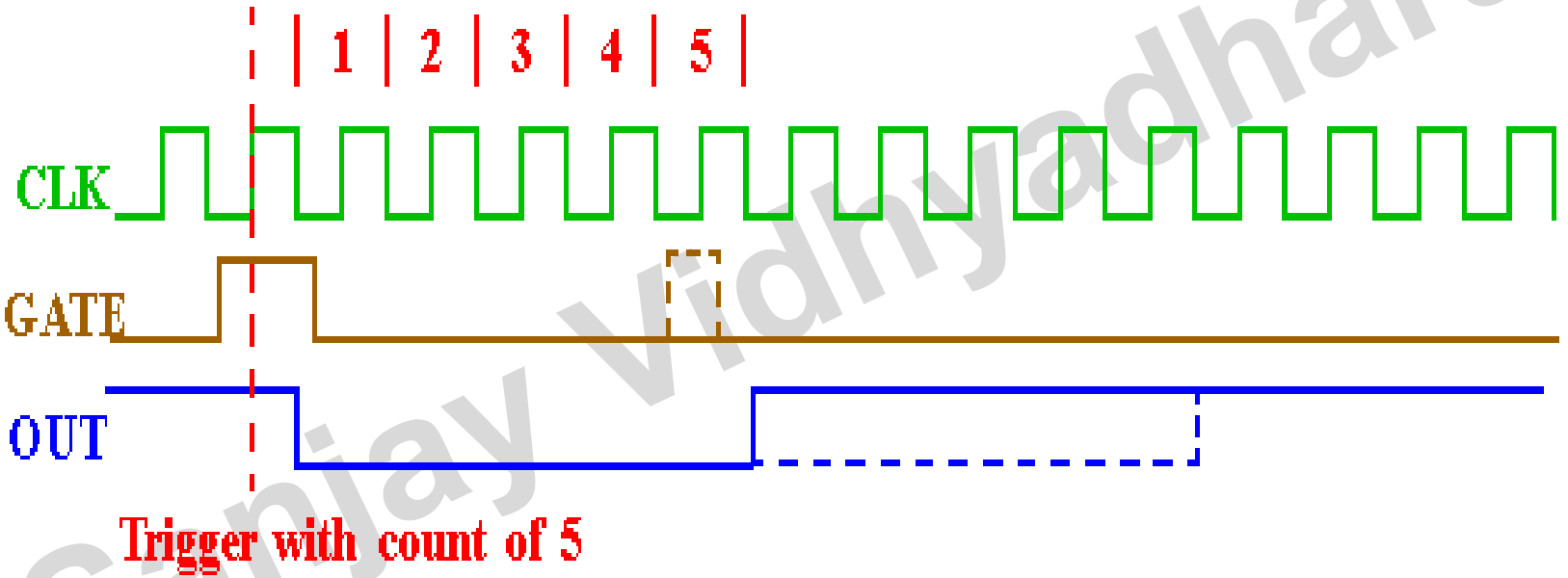
- A +ve transition at gate reloads the counter & countdown begins afresh

Mod 1: Case 3



- A new count is not loaded till gate is triggered

Modes of counting : Mode 1



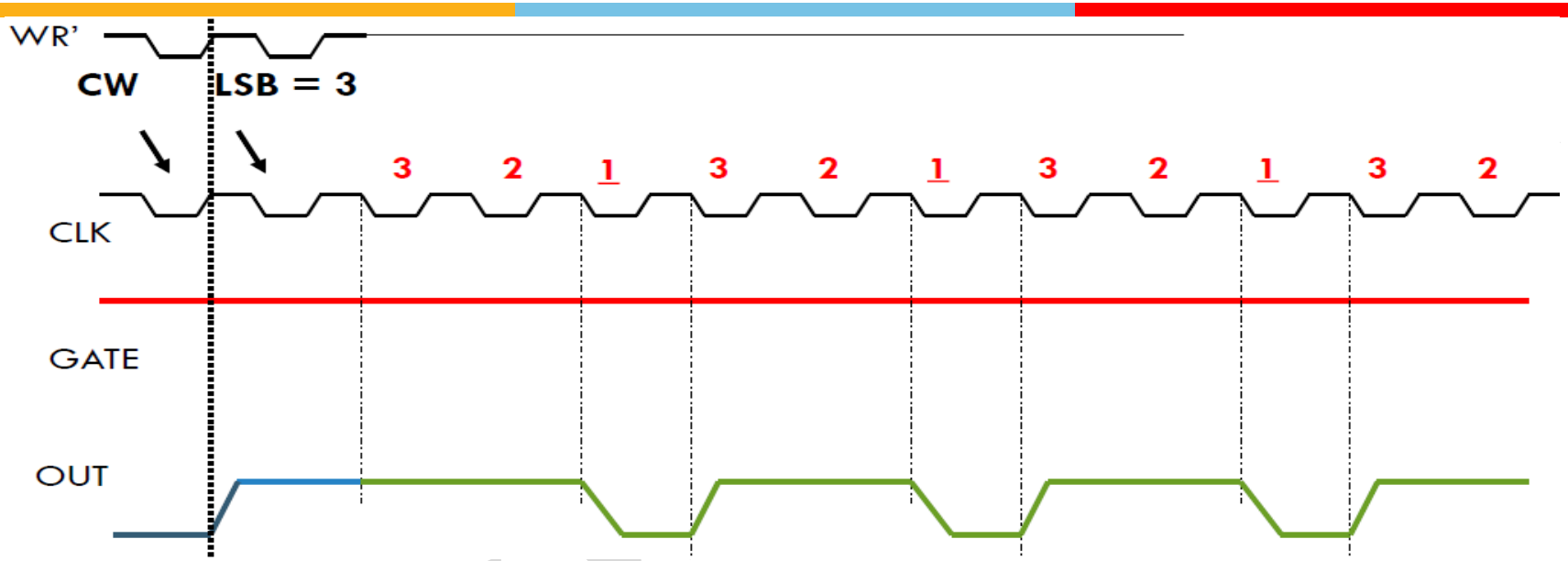
Mode 2
Rate Generator (Divide by N counter)

1. Output is low for one clock.
2. Again low after TC
3. If count is loaded, current rate not effected but next rate changes.
4. Low gate input forces output high.
5. Gate input when high starts counting.
6. Gate input used as synchronizer.

Use:

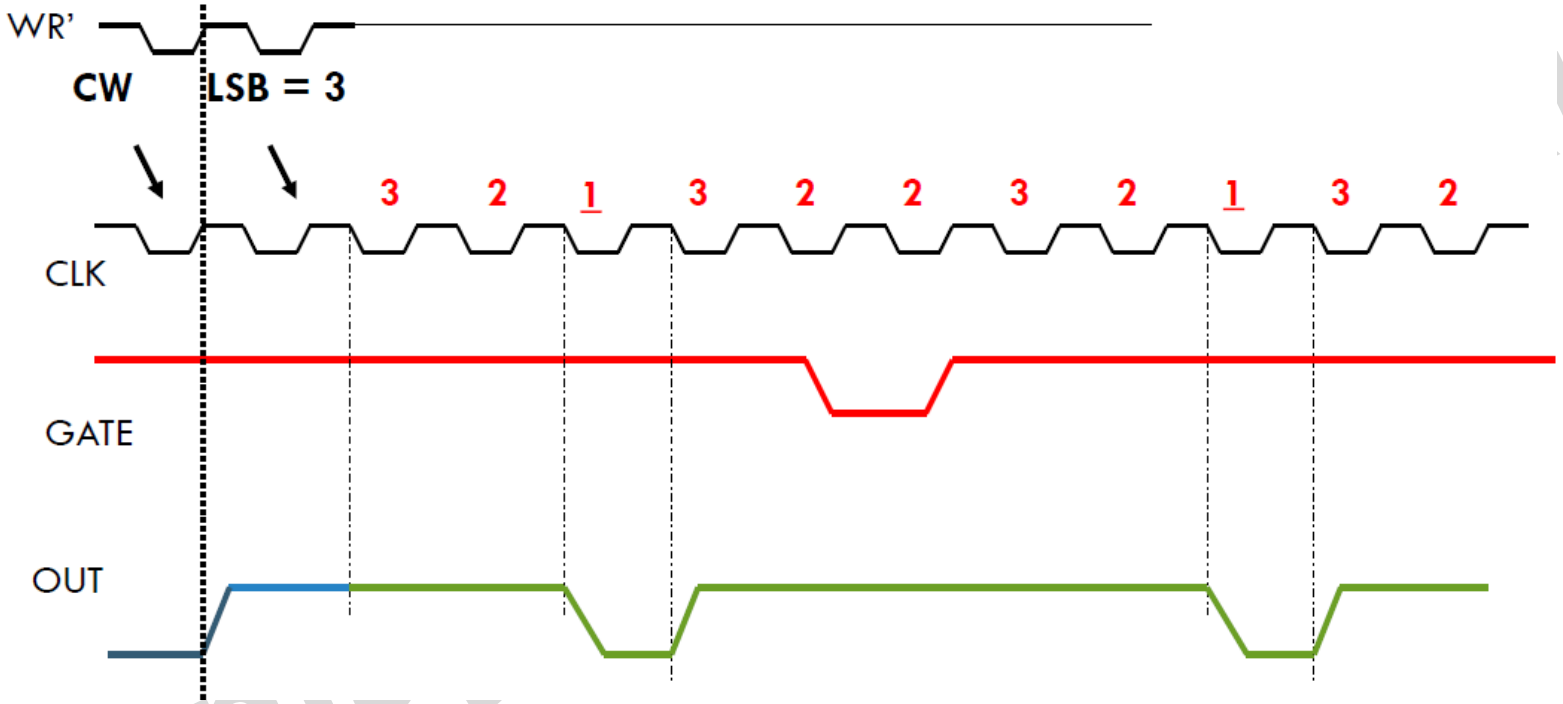
1. Programmable pulse sequence generator.
2. Use the output to trigger periodic events at programmable rate.
3. Programmable pulse width generator

Case 1



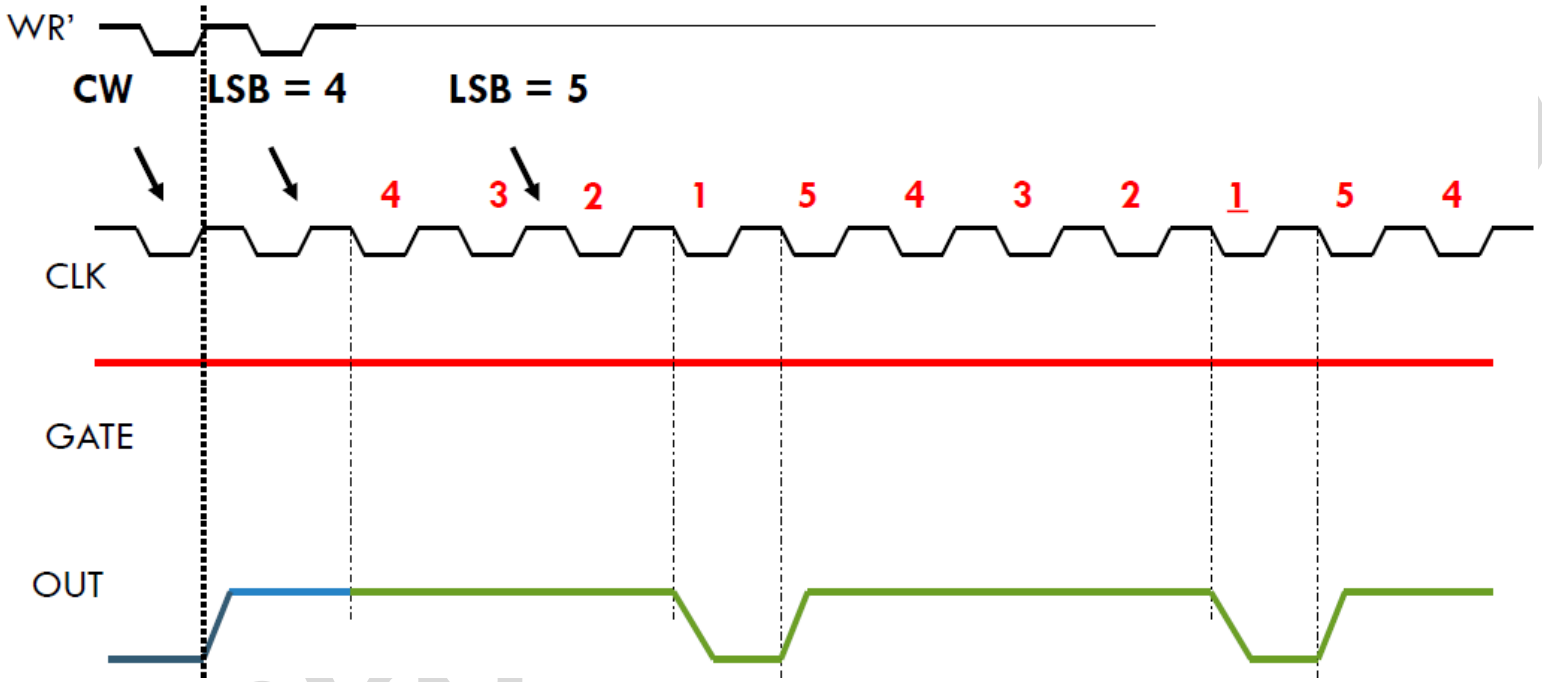
- Countdown starts one clock cycle after the gate is made high (or one cycle after the count is written if gate is already high)
- On reaching a count of one, the OUT goes low for one cycle. If the counter is loaded with a number N, then OUT pin will go low for one clock cycle every N input clock pulses.
- Now count is automatically reloaded and whole process repeats

Case 2



- If gate is made low during countdown then counting stops and OUT is made immediately high

Case 3

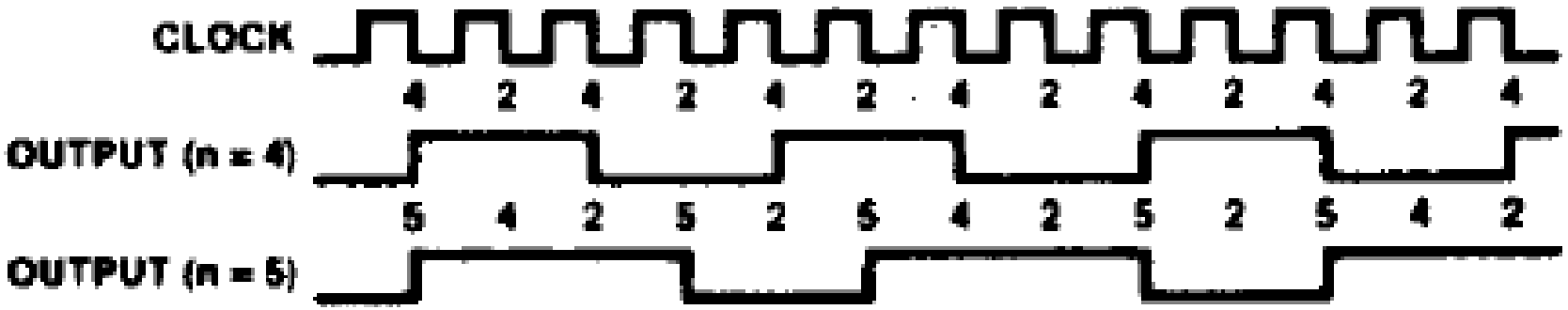


- If a new count is written then it is loaded only after previous countdown finishes

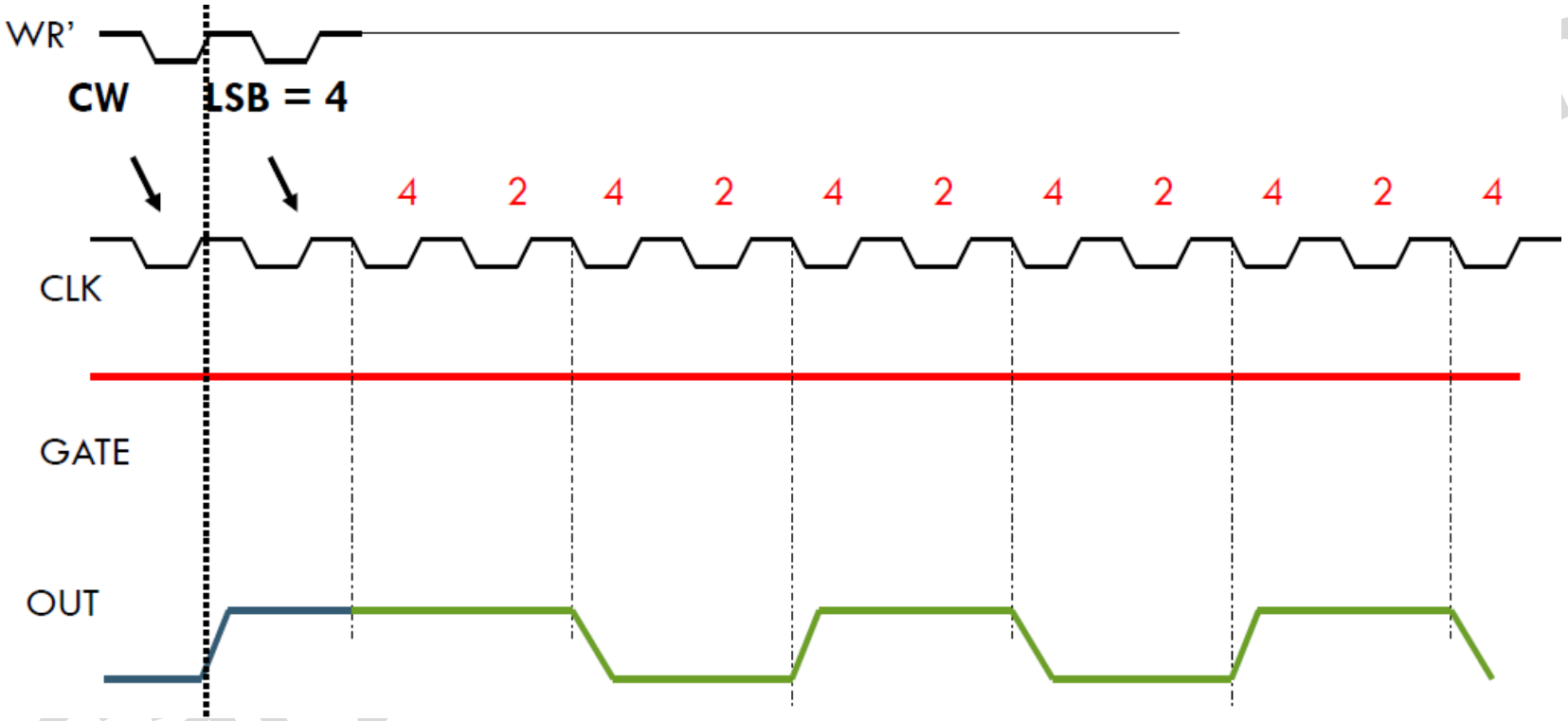
Mode 3 -Square Wave Generator

1. Same as mode 2 but generates square wave with 50% period.
2. If count is odd you get (N+1)/2 and (N-1)/2 as period.

Use:
Programmable square wave generator

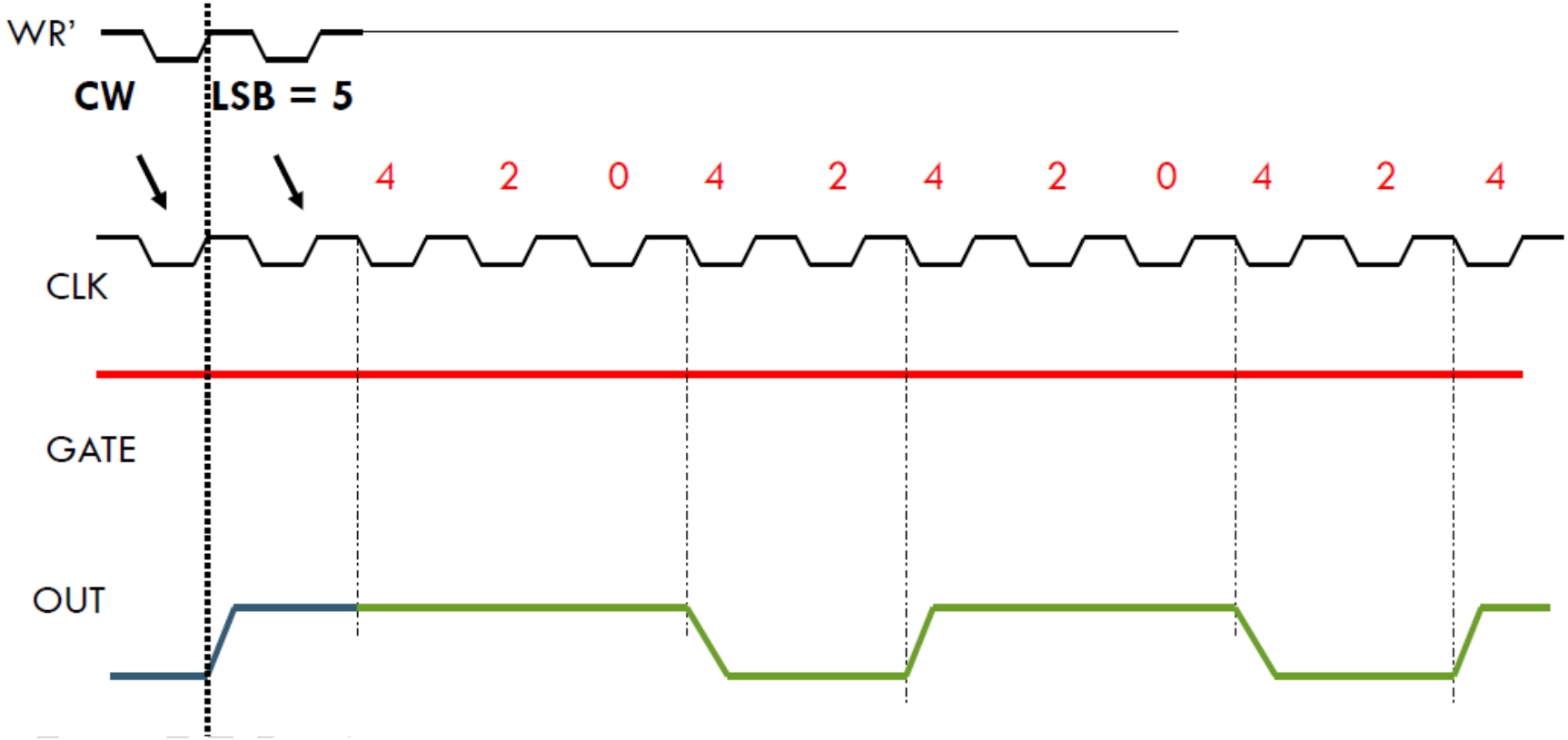


Case1 :Even count



- Each clock pulse decrements the counter by 2
- Count is automatically reloaded on 2

Case2 :Odd count

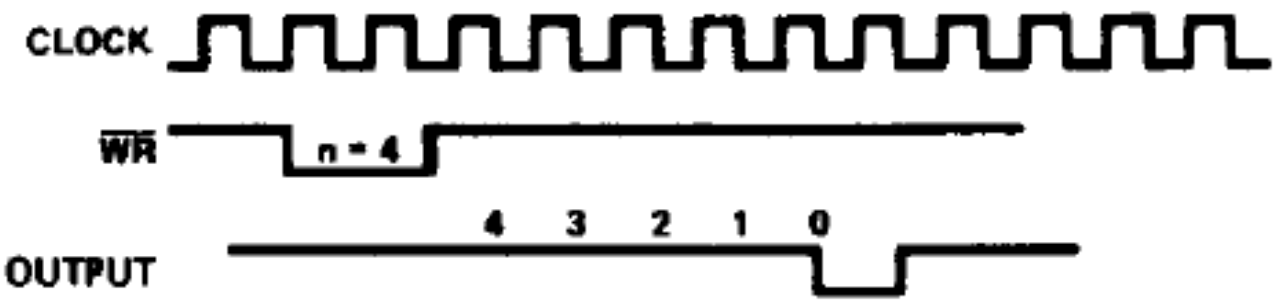


- If gate is made low during countdown then counting stops and when gate is made high again, counting continues.

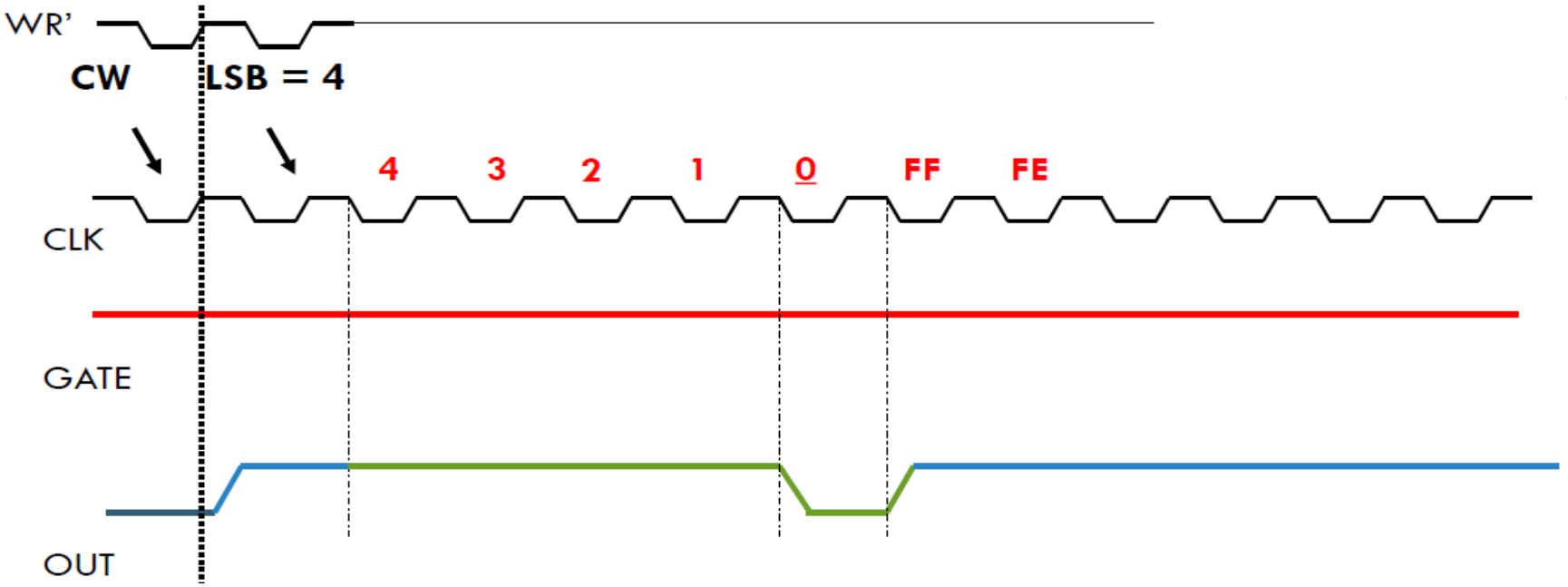
Mode 4 – Software triggered strobe

1. Similar to Mode 0.
2. This generates a single clock pulse after TC rather creating an edge after TC.
3. Count disabled when gate is low.

Use:
1. Create periodic triggers to strobe peripherals
2. Create periodic interrupts

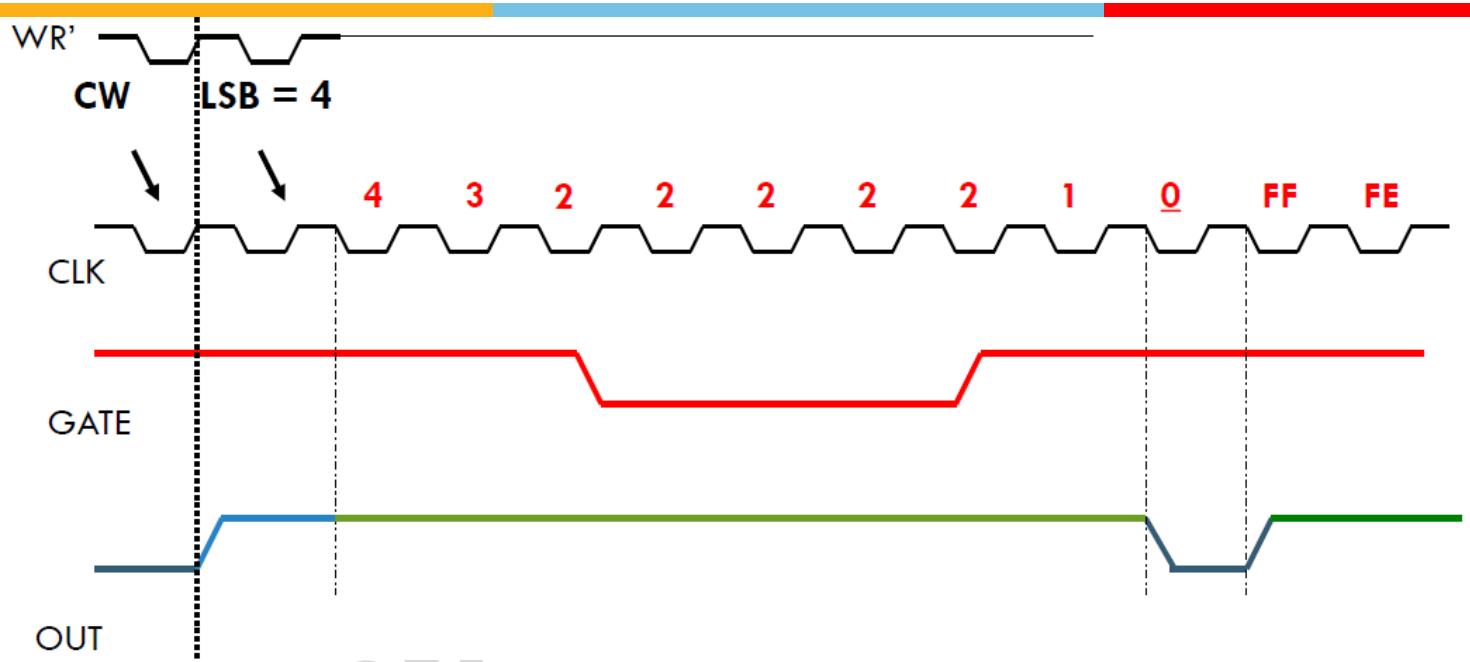


Case1



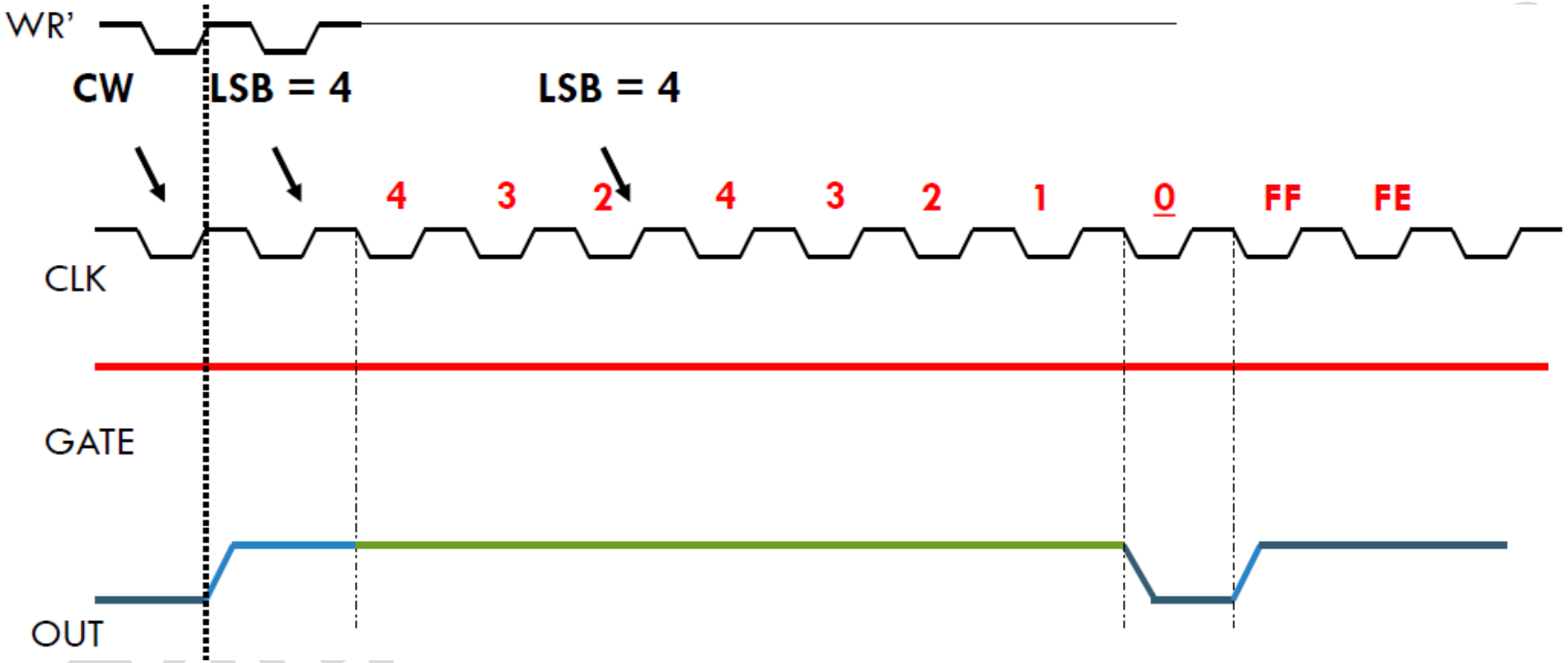
- If GATE =1, OUT goes low N+1 cycles after the count is written.
- OUT is low for one clock cycle
- Count must be reloaded to repeat the strobe
- not automatically reloaded

Case 2



- If GATE→low, the OUT → high and count stops; count resumes (from where it stopped) when GATE→high

Case 3



- Count must be reloaded to repeat the strobe

Mode 5 – Hardware triggered strobe

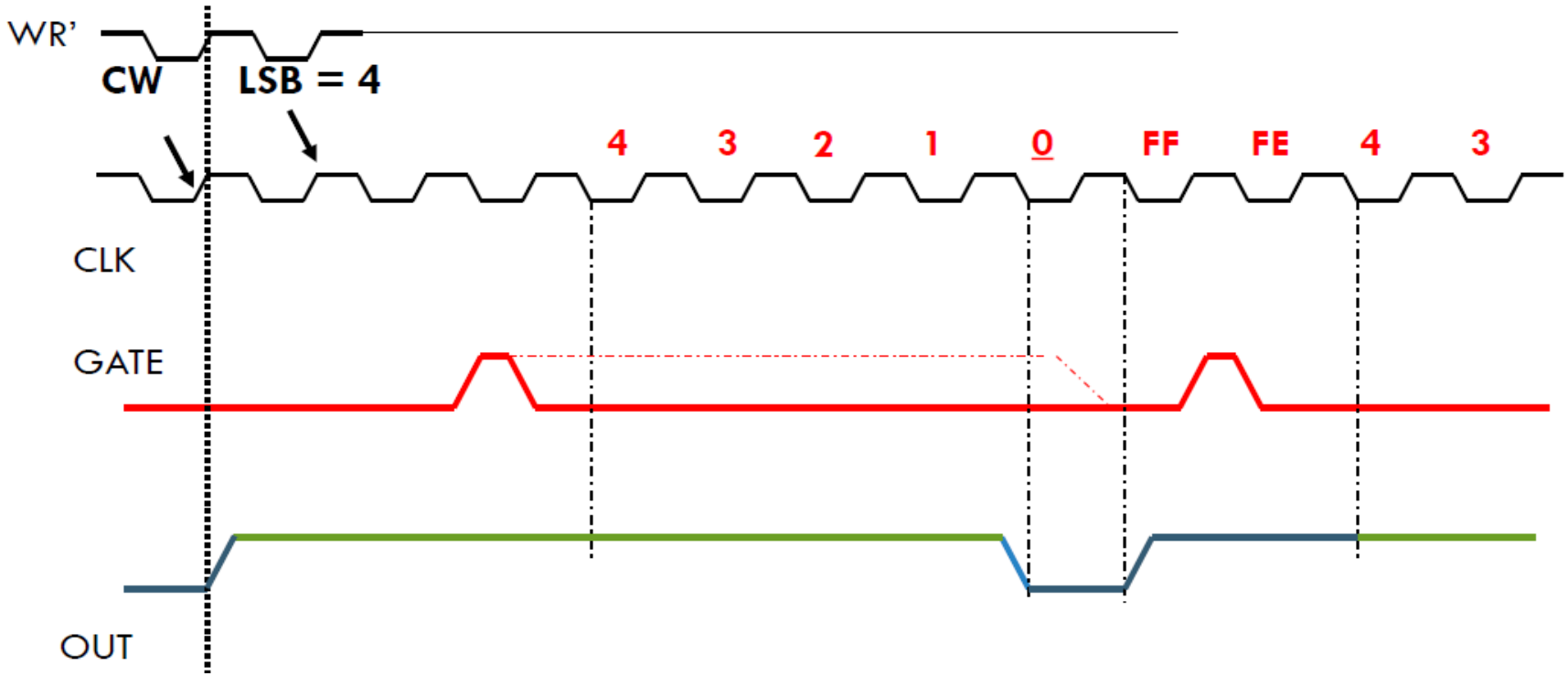
1. Starts counting after count is loaded and gate is high.
2. Counter retriggerable
3. Same as Mode 4 but the strobe is generated with respect to the gate.

Use:

1. When you want to generate an event from a random event.

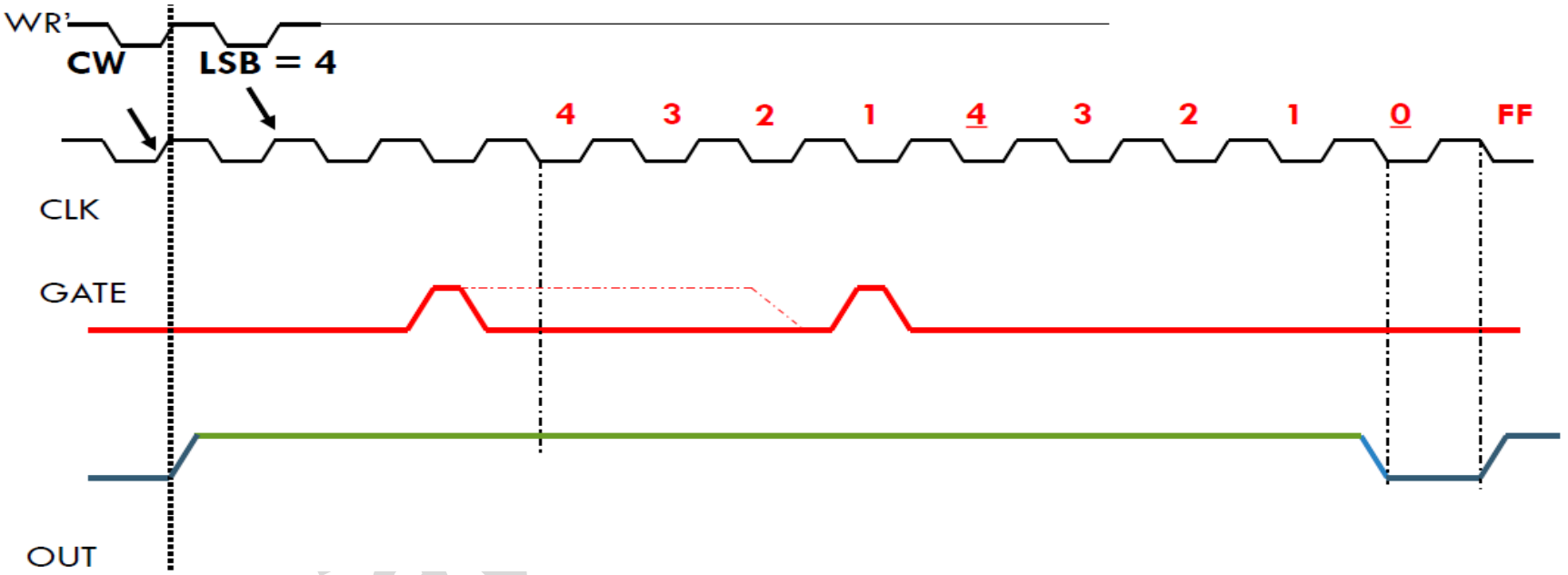
I/O handshake

Case 1



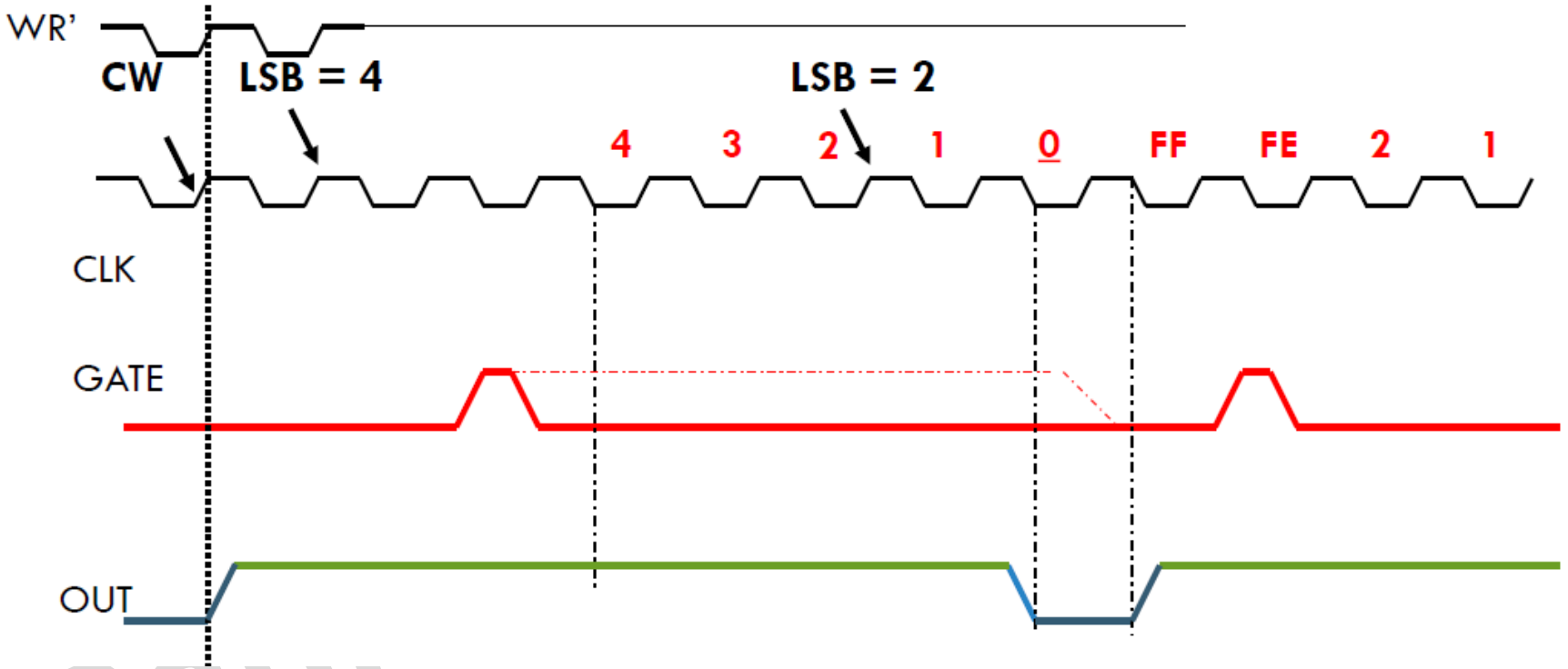
- Like mode 4, but triggering is done with GATE instead
- Count begins when 0-1 pulse hits GATE
- OUT goes low N+1 cycles after gate is triggered.
- OUT is low for one clock cycle

Case 2



- Gate must be triggered again to repeat the strobe
- A trigger on gate in between countdown will reload the count and keep OUT high

Case 3

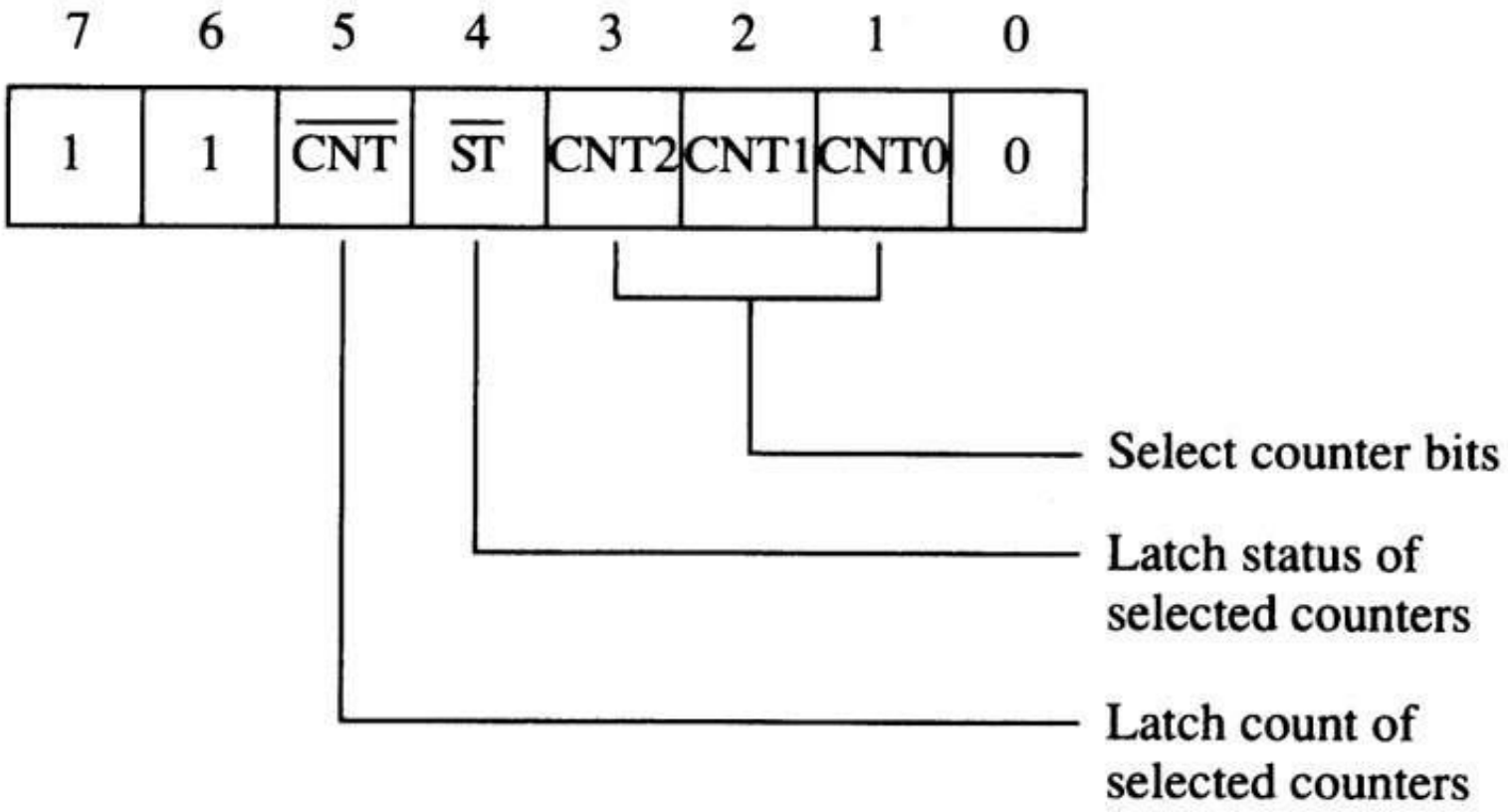


- not automatically reloaded
- If GATE→low, it does not stop countdown

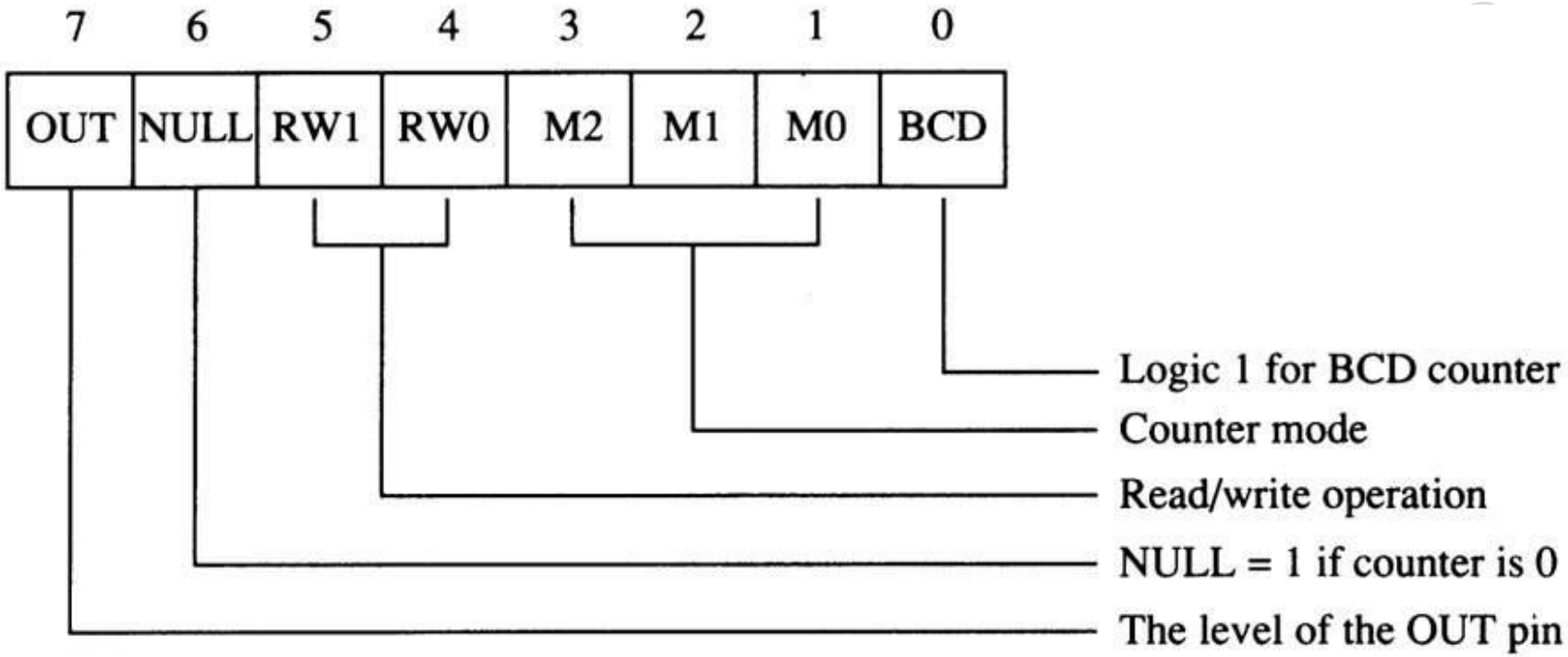
Reading the counter values

- 8254 counters have latches on their outputs. Normally enabled during counting, so that latch outputs follow counter outputs.
- When reading the current count value, we read data on outputs of these latches.
- For reading the correct count….Counting must be stopped.
- Can be done by removing clock, gate etc…….but not preferred as requires extra hardware..
- Latch the count before reading…..by
- Sending counter latch command word at CR (A_1 A_0 =11) and then read.

8254 Read Back control word



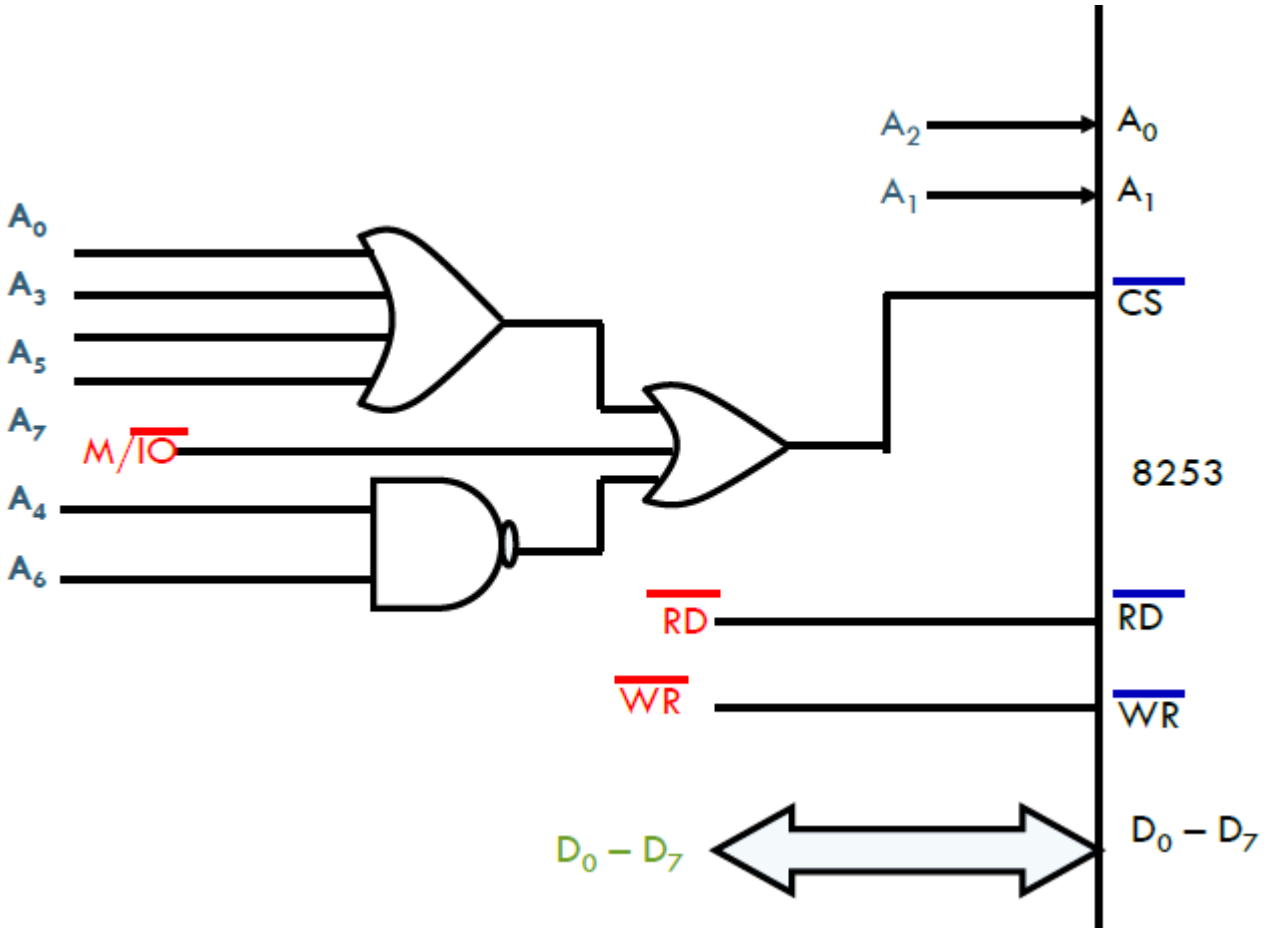
Status Register(8254 only)



Example :1

Draw the interface diagram and write a program for 8253 interface starting at 50H,
Counter 0 used in mode 1, MSB+LSB, binary, to be loaded with 3080H
Counter1 used in mode 0, LSB only, BCD to be loaded with 99.

Example:1

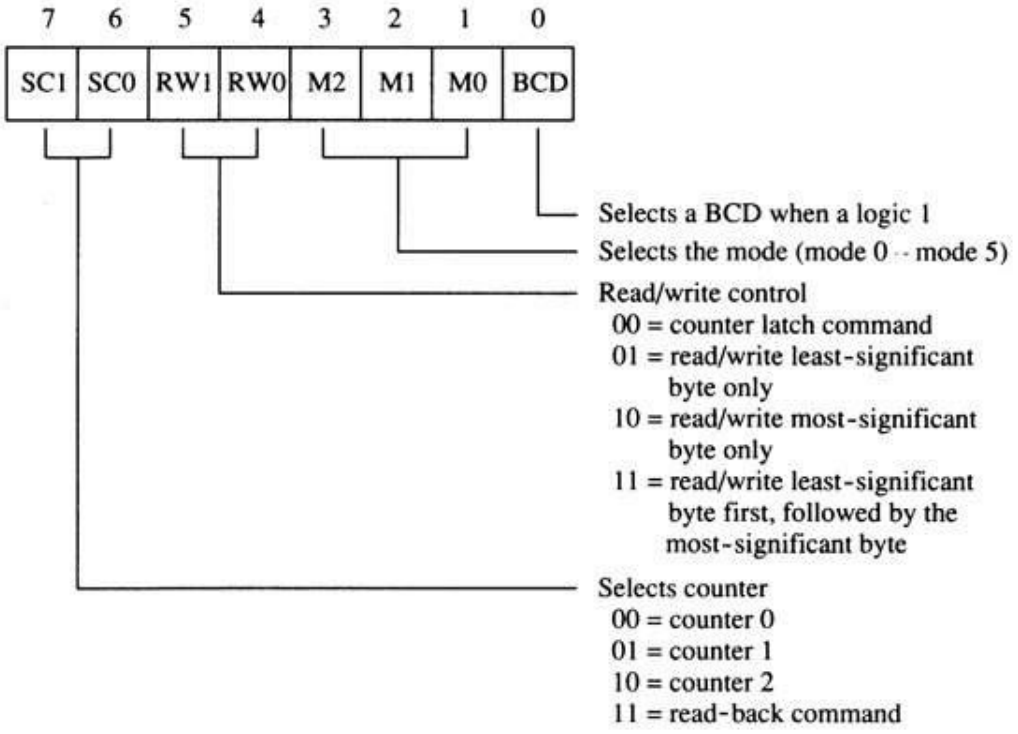


Example:1

Counter 0 used in mode 1, MSB+LSB, binary, to be loaded with 3080H
Counter1 used in mode 0, LSB only, BCD to be loaded with 99.

Control word1=00110010 – 32H
Control word2=01010001-51H

```
CNT0 EQU 50H
CNT1 EQU 52H
CR EQU 56H
MOV AL, 32H
OUT 56H, AL
MOV AL, 51H
OUT 56H, AL
MOV AL, 80H
OUT 50H, AL
MOV AL, 30H
OUT 50H, AL
MOV AL, 99
OUT 52H, AL
```



Example :2

Design a programmable timer using 8254 and 8086. Interface 8254 at an address 0040H for counter 0 and write the following ALPs. The 8086 and 8254 run at 6 MHz and 1.5 MHz respectively.

(i) To generate a square wave of period 1 ms.

(ii) To interrupt the processor after 10 ms.

(iii) To derive a monoshot pulse with quasistable state duration 5 ms.

Example :2

For generating a square wave, 8254 should be used in mode 3.

$f = 1.5$ MHz,

$$\Rightarrow \quad T = \frac{1}{1.5\times10^{-6}} = 0.66\,\mu s$$

If N is the number of T states required for 1ms,

$$N = \frac{1\times10^{-3}}{0.66\times10^{-6}} = 1.5\times10^{3}$$
$$= 1500 \text{ states}$$

The control word is decided as below:

SC1	SC0	RL1	RL0	M2	M1	M0	BCD
0	0	1	1	0	1	1	1

= 37 H

The ALP is given in Program 6.1.

```
CODE        SEGMENT
ASSUME      CS : CODE
START:      MOV AL,37H          ; Initialize 8254,
            OUT 46H,AL          ; counter 0 in mode3.
            MOV AL, 00          ; Write 00 decimal
            OUT 40H, AL         ; in LSB of count reg. and
            MOV AL, 15          ; 15 decimal in MSB as a
            OUT 40 H, AL        ; count.
            MOV AH,4CH
            INT 21H
 CODE       ENDS
            END START
```

Example :2

(ii) For generating interrupt to the processor after 10 ms, the 8254 is to be used in mode 0. The OUT1 pin of 8254 is connected to interrupt input of the processor. Let us use counter 1 for this purpose, and operate the 8254 in HEX count mode.

No. of T states required for 10 ms delay $= \dfrac{10 \times 10^{-3}}{0.66 \times 10^{-6}} = 15 \times 10^{3}$

$= 15000$

$= 3A98$ H

The Control word is written below:

SC1	SC0	RL1	RL0	M2	M1	M0	BCD
0	1	1	1	0	0	0	0

$= 70$ H

The ALP is written in Program 6.2.

```
CODE        SEGMENT
ASSUME      CS : CODE
START:      MOV AL, 70 H        ; Initialize 8254 with
            OUT 46H, AL         ; Counter1 in mode 0.
            MOV AL, 98H         ; Load 98H as LSB of count
            OUT 42H, AL         ; in count reg of counter1
            MOV AL. 3AH         : then load 3AH in MSB

            OUT 42H, AL         ; of counter1
            MOV AH,4CH          ; RETURN TO DOS
            INT 21H             ;
CODE        ENDS
            END START
```

Example :2

(iii) For generating a 5 ms quasistable state duration, the count required is calculated first. The counter 2 of 8254 is used in mode 1, to count in binary. The OUT2 signal normally remains high after the count is loaded, till the trigger is applied. After the application of a trigger signal, the output goes low in the next cycle, count down starts and whenever the count goes zero the output again goes high.

Number of T states required for 05 ms $= \dfrac{5 \times 10^{-3}}{0.66 \times 10^{-6}} = 7500$ states

$= 1\ D4C\ H$

The Control word is written below:

SC1	SC0	RL1	RL0	M2	M1	M0	BCD
1	0	1	1	0	0	1	0

$= B2\ H$

The ALP for the above purpose is written in Program 6.3.

```
CODE        SEGMENT
ASSUME      CS : CODE
START:      MOV AL, B2 H        ; Initialize 8254 with
            OUT 46H, AL         ; Counter 2 in mode 1
            MOV AL, 4CH         ; Load 4CH (LSB of count)
            OUT 44H, AL         ; into count register
            MOV AL, 1D          ; Load 1 DH (MSB of count)
            OUT 44H, AL         ; into count register
            MOV AH, 4CH         ; Stop
            INT2IH
CODE        ENDS
            END START
```

Thank You