Microprocessors and Interfaces: 2021-22
Lecture 29 :
8253/8254 Timer
Part:1

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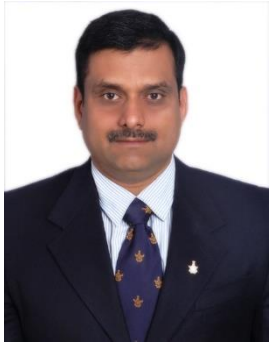
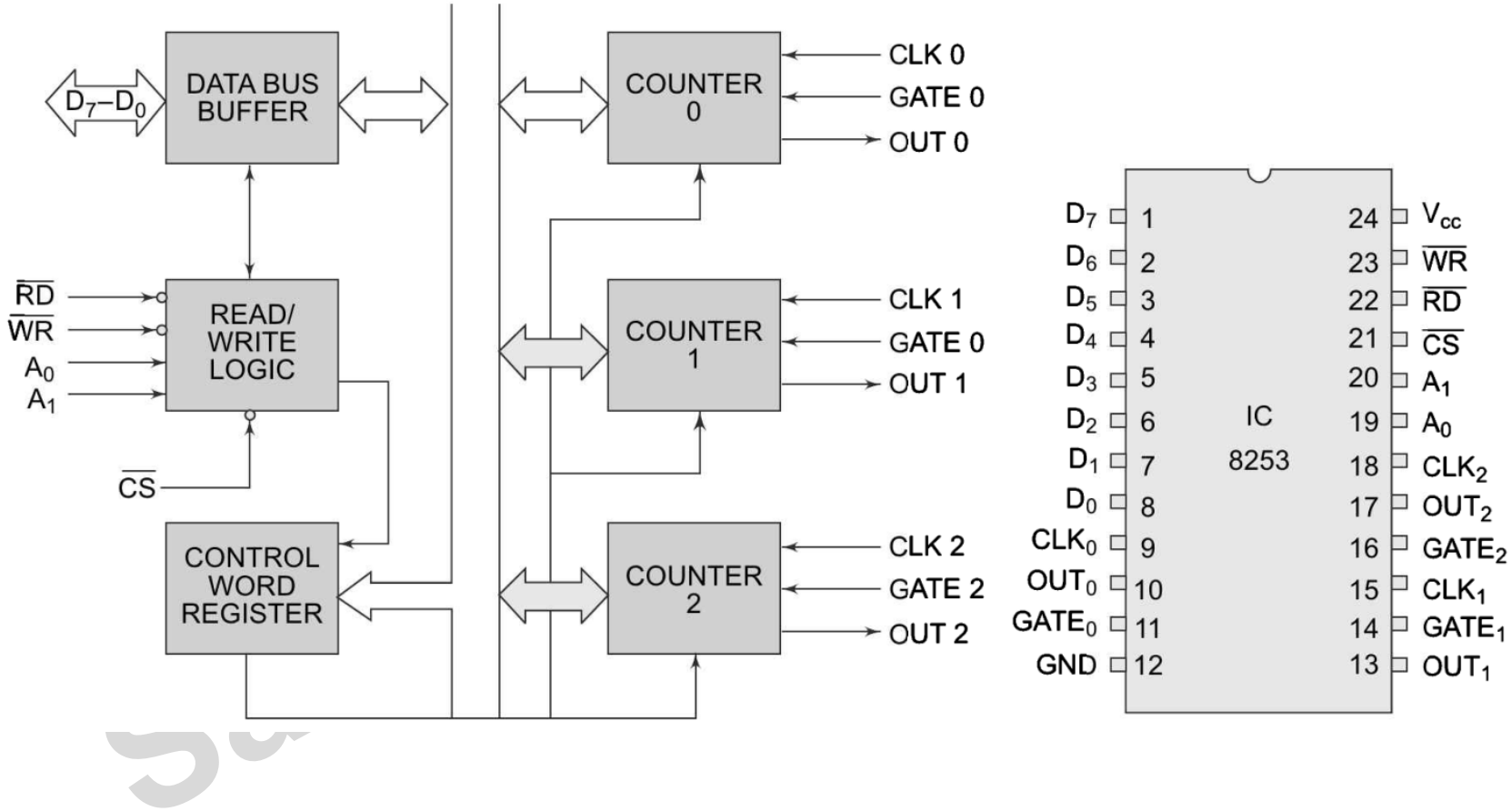


Features of 8253/8254

- The 8254 consists of three independent 16-bit programmable counters (**timers**).
- Each counter is capable of counting in binary or binary-coded decimal (BCD).
- Maximum allowable input frequency to any counter is 10 MHz
- Useful where the microprocessor must control real-time events. Ex: real-time clocks, event counters, and motor speed/direction control.

8253	8254
Its operating frequency is 0 - 2.6 MHz	Its operating frequency is 0 - 10 MHz
It uses N-MOS technology	It uses H-MOS technology
Read-Back command is not available	Read-Back command is available

Pin diagram of 8253/8254



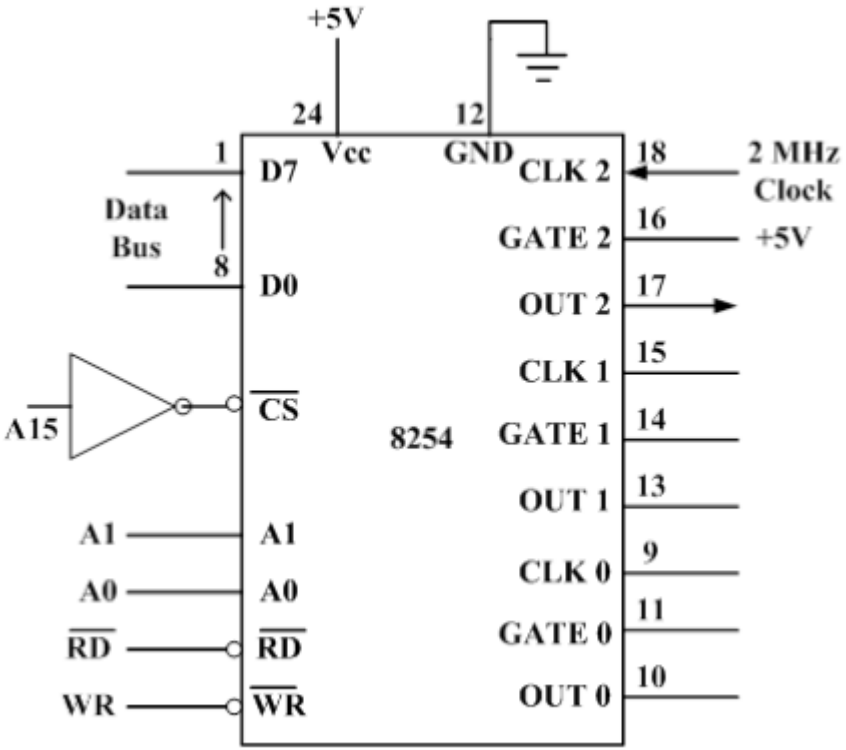
Features of 8253/8254

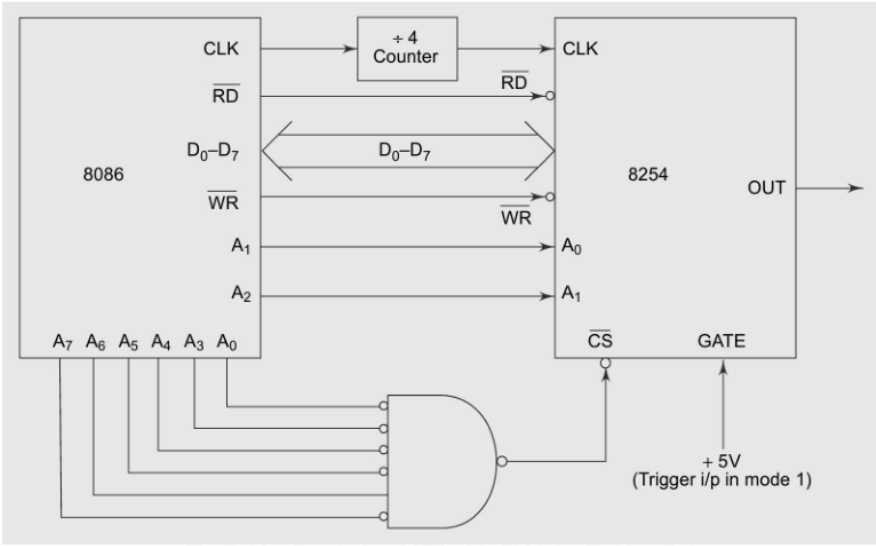
- **Each timer contains:**
  - a **CLK** input which provides the basic operating frequency to the timer
  - a **Gate** input pin which controls the timer in some modes.
  - an **output** (OUT) connection to obtain the output of the timer.

Memory mapping

CS'	A_1	A_0	Selected
0	0	0	Counter 0
0	0	1	Counter 1
0	1	0	Counter 2
0	1	1	Control Register
1	X	X	8253/8254 Not Selected

Control word Format



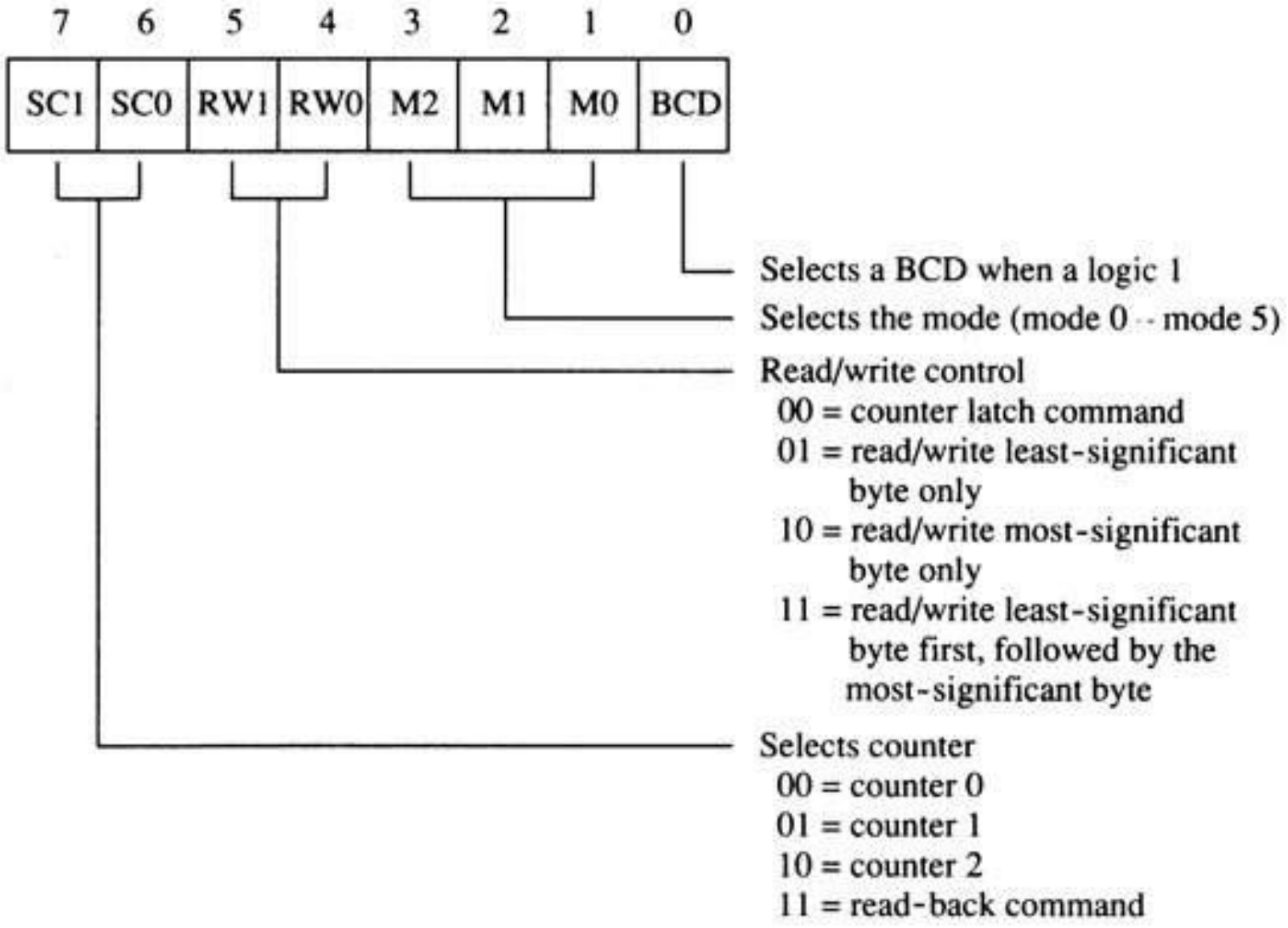


Programming the Counters

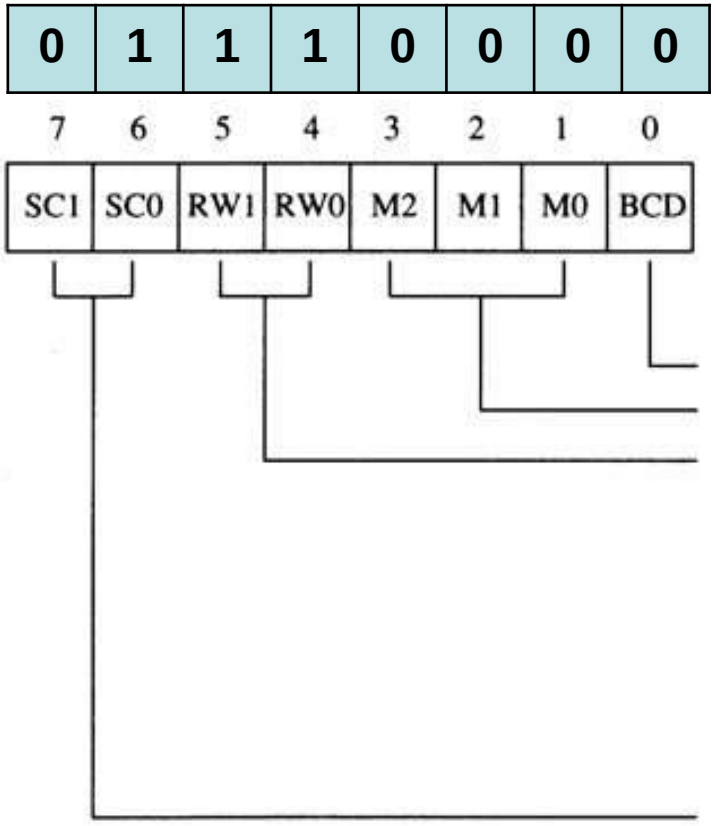
Before you can use……

1. Initialize the mode of every counter planned to be used
2. This is done by sending individual command words for every counter
3. These CWs are sent at A_1A_0 =11
4. Send counts to the counters
5. This is done at counter addresses
6. Enable gates for counting to start

Control word Format



Control word Format



Counter-1 Mode 0, Binary, N= 3A98H

```
MOV AL, 70 H        ; Initialize 8254 with
OUT 46H, AL         ; Counter1 in mode 0.
MOV AL, 98H         ; Load 98H as LSB of count
OUT 42H, AL         ; in count reg of counter1
MOV AL. 3AH         : then load 3AH in MSB
OUT 42H, AL       ; of counter1
```

Only 98H in LSB of Counter-1

Mov AL, 50H;
OUT 46H, AL
MOV AL, 98H
OUT 42H, AL

Only 3AH in MSB of Counter-1

Mov AL, 60H;
OUT 46H, AL
MOV AL, 3AH
OUT 42H, AL

Reading the Counters

Simple Read Operation

Counter selected with the A1, A0 inputs, the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result. Two I/O read operation are performed by the MPU

1. The first I/O operation reads the low order byte.
2. The second I/O operation reads high order byte.

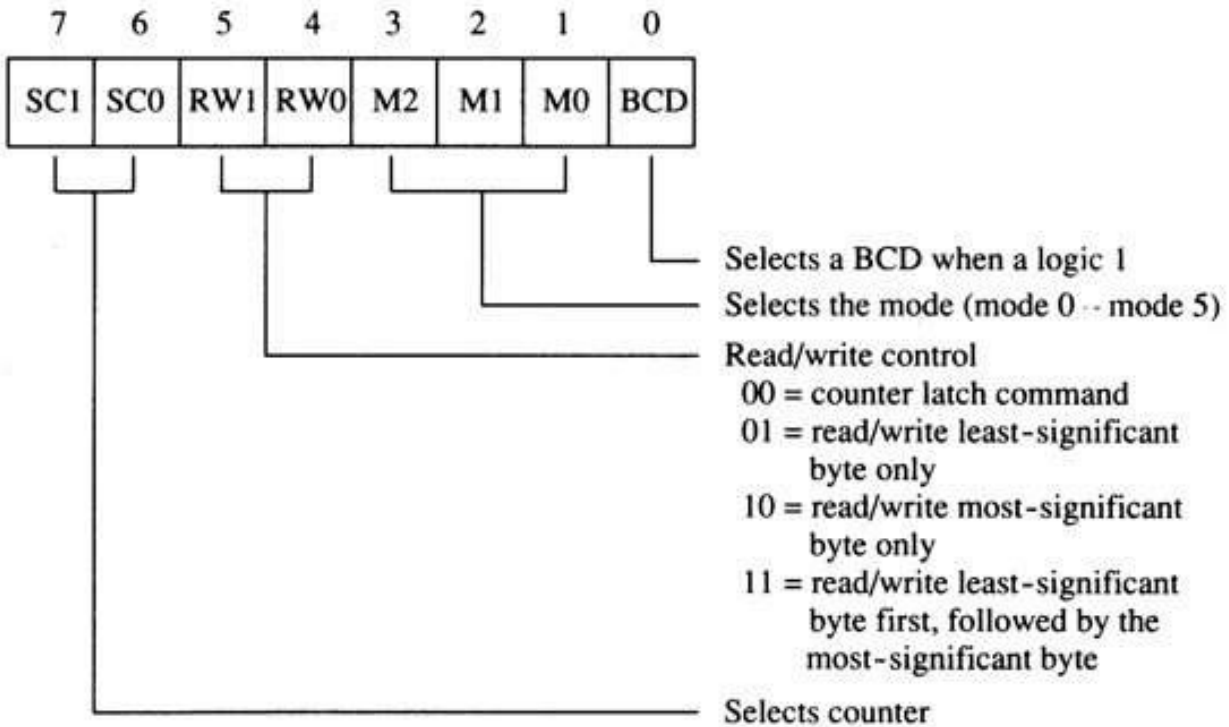
Counter Latch Command

This allows reading the contents of the Counters “on the fly" without affecting counting in progress.

The selected Counter's output latch (OL) latches the count at the time the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to “following" the counting element (CE).

Reading the Counters

Counter Latch Command



Latching counter0

```
MOV DX, C_REG
MOV AL, 00000000B ;
OUT DX, AL
```

Reading counter0

```
MOV DX, CNTR0
IN AL, DX
```

A_1,A_0 = 11; CS = 0; RD = 1; WR = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

Read-Back Command

This command is used to read several counters at a time. It eliminates the need of writing separate counter-latch commands for different counters.
It allows the user to check the count value, programmed Mode, and current states of the OUT pin and Null Count flag of the selected counter/ counters.
The read back command is written to the Control Word Register.
is reprogrammed). The counter is automatically unlatched when read, but other counters remain latched until they are read.

A0, A1 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT 2	CNT 1	CNT 0	0

D_5: 0 = Latch count of selected counter(s)
D_4: 0 = Latch status of selected counters(s)
D_3: 1 = Select Counter 2
D_2: 1 = Select Counter 1
D_1: 1 = Select Counter 0
D_0: Reserved for future expansion; Must be 0

Figure Read-Back Command Format

Read-Back Command

The read-back command may be used to latch multiple counter output latches (OL) by setting the COUNT bit D5 =0 and selecting the desired counter(s).

A single read back command is functionally equivalent to several counter latch commands.

Each counter's latched count is held in the OL until it is read (or the counter is reprogrammed). The counter is automatically unlatched when read, but other counters remain latched until they are read.

The read-back command may also be used to latch status information of selected counter(s) by setting STATUS bit D4 = 0. Status must be latched to be read; status of a counter is accessed bv a read from that counter.

The counter status format is shown in Figure below.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Output	Null Count	RW1	RW0	M2	M1	M0	BCD

D_7 1 = OUT Pin is 1
0 = OUT Pin is 0

D_6 1 = Null Count
0 = Count available for reading

D_5–D_0 Counter programmed mode

Read-Back Command

Example:

Count and Status latched for counter 0
MOV DX, C_REG
MOV AL, 11000010B ; count latched for counter 0
OUT DX, AL

Reading the latched status for count 0
MOV DX, TRM0
IN AL, DX ; Reading Status
MOV AH, AL
Reading the latched count for counter 0
IN AL, DX ; Reading LSB of counter 0
MOV BL, AL
IN AL, DX ; Reading MSB of counter 0
MOV BH, AL

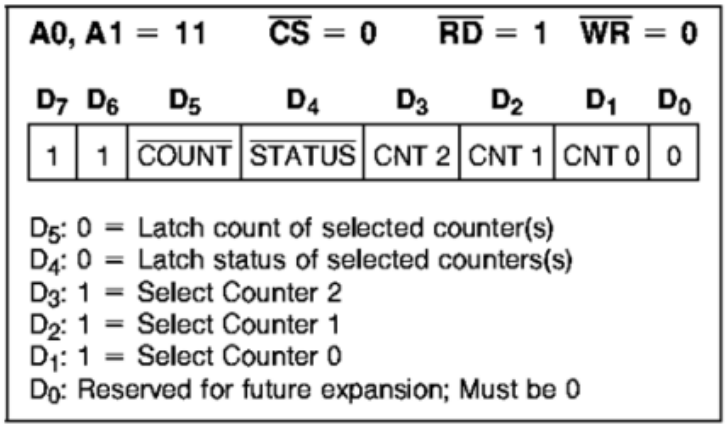


Figure Read-Back Command Format

Control word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

Selects Counter

00	Counter 0
01	Counter 1
10	Counter 2
11	Read Back Command

Read/Write Control

00	Latch Counter
01	R/W LSB
10	R/W MSB
11	R/W LSB followed by MSB

Timer Mode

000	Interrupt on T/C
001	h/w re-Triggerable one shot
010	rate generator
011	Square wave generator
1x0	s/w triggered strobe
1x1	h/w triggered strobe

0 – binary 0000_h $FFFF_h$

1 – BCD 0000 9999

Programming of 8253/8254

- Each counter is programmed by writing a control word, followed by the initial count.

➢ The control word allows the programmer to select

- the counter,
- mode of operation, and
- type of operation (read/write).
- also selects either a binary or BCD count

Mode of Operation

–Six modes (Mode 0–Mode 5) of operation are available to each of the 8254 counters

–each mode functions with the CLK input, the gate (G) control signal, and OUT signal.

Modes of counting

- Interrupt on terminal count
- Programmable one shot
- Square wave generator
- Rate generator
- Software triggered strobe
- Hardware triggered strobe

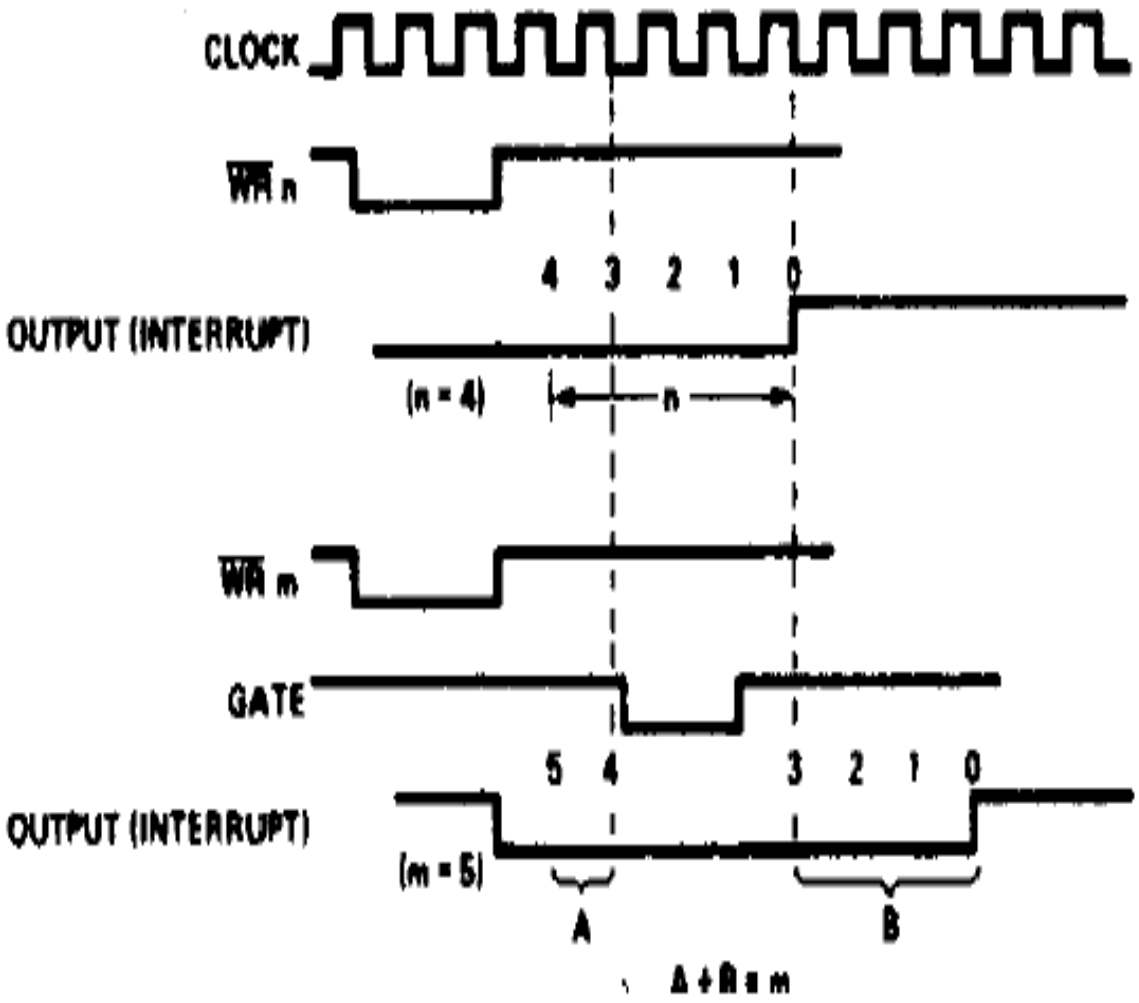
Mode 0 –Interrupt on Terminal count

- **Interrupt on terminal count (event counter)**
- Out pin goes low when mode word or new count is written
- Now if clock is applied and gate=1, countdown begins
- Countdown stops if gate=0: resumes if gate=1
- If count written is N then OUT becomes high after N+1 clocks
- OUT remains high till a new count is written
- Countdown continues as FF_H, FE_H if gate =1
- Application – object counting

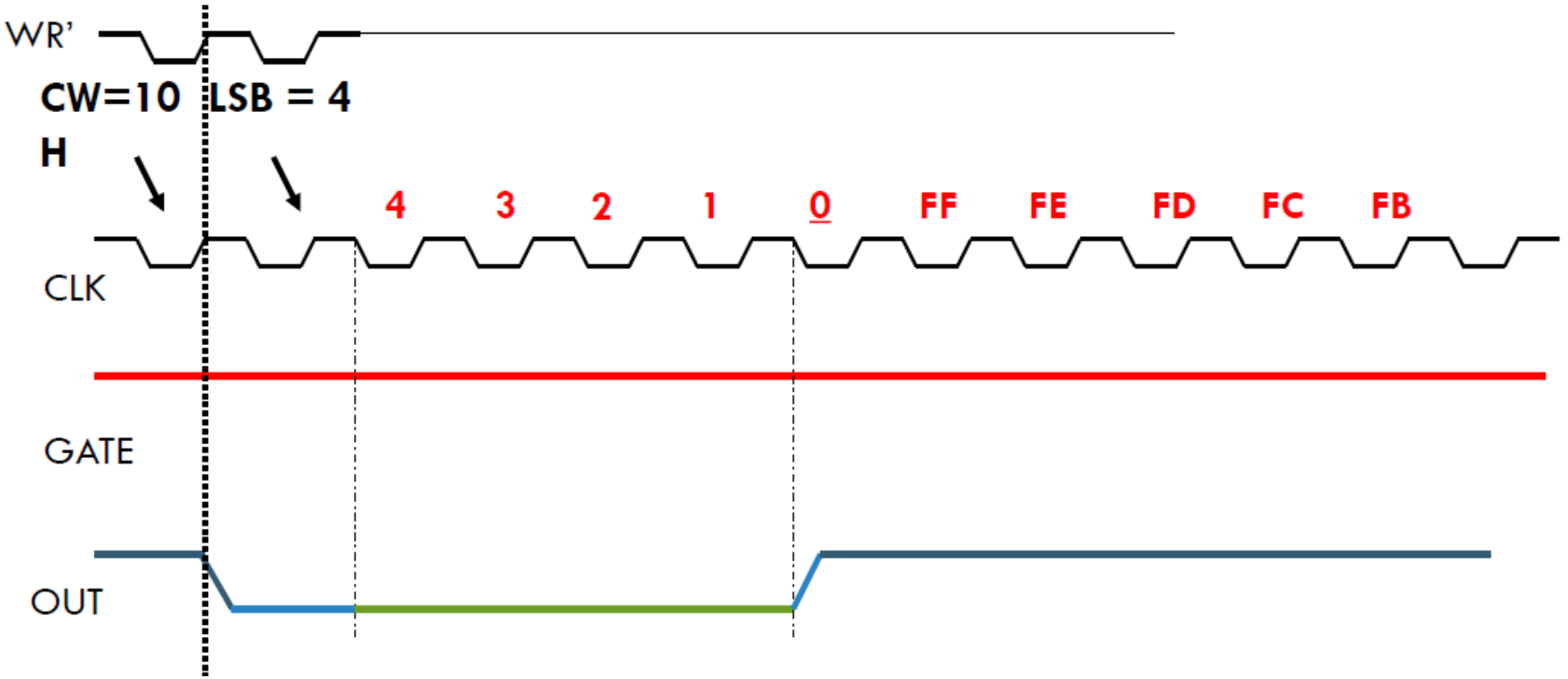
Mode 0 –Interrupt on Terminal count

- Output goes high when TC is reached.
- Remains high till counter is re-loaded
- Writing first byte stops counting.
- Writing second byte starts new count.

use:
1. Self generated interrupt.
2. Programmable delayed event.

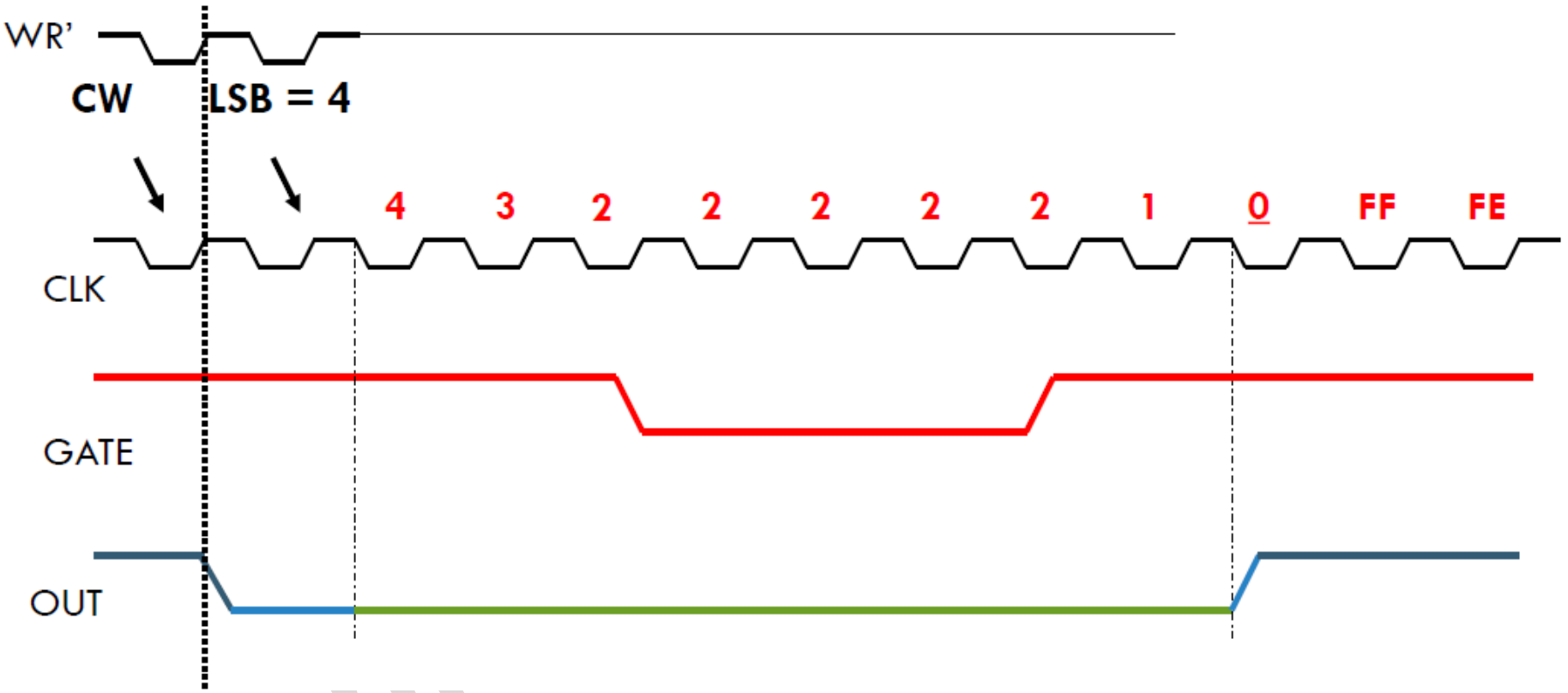


Mod 0 : Case 1



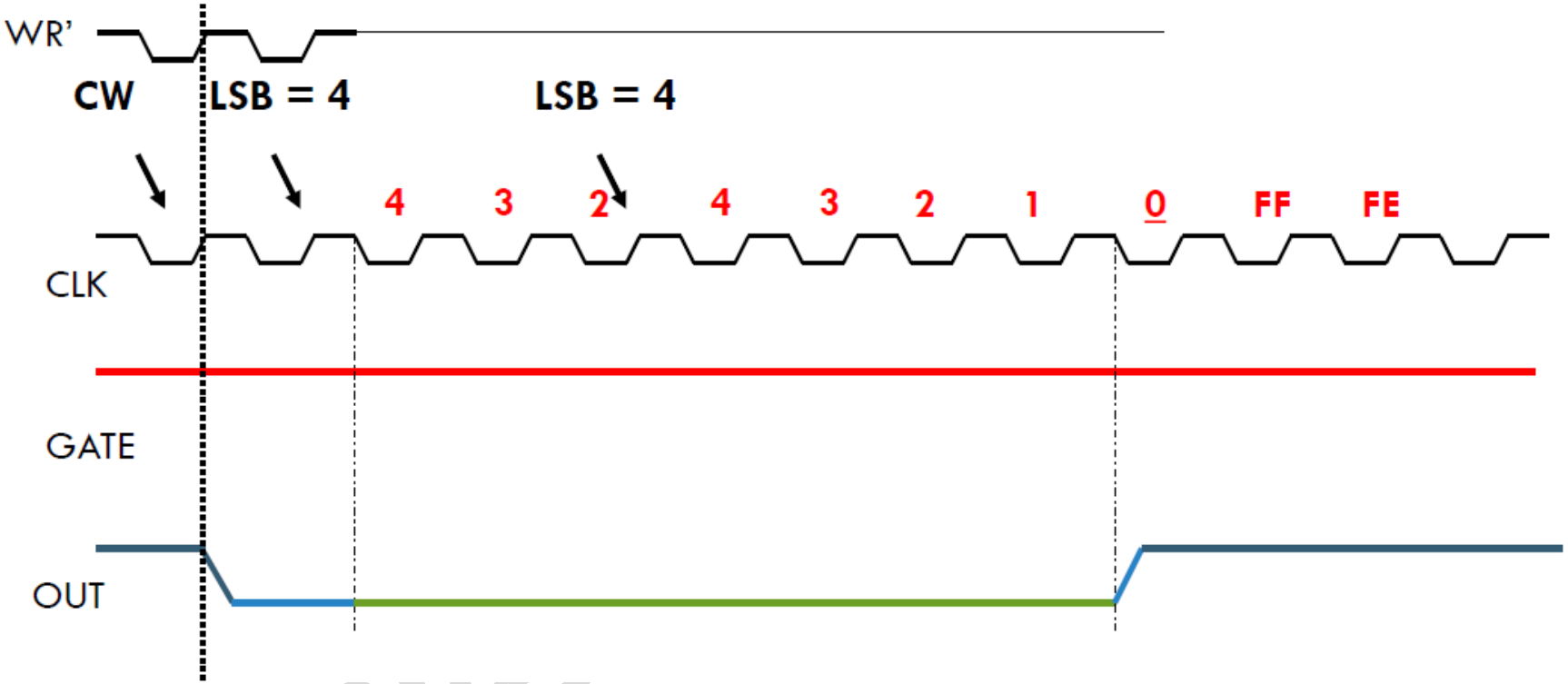
- Out pin goes low when mode word or new count is written
- Now if clock is applied and gate=1, countdown begins
- If count written is N then OUT becomes high after N+1 clocks

Mod 0 : Case 2



- Countdown stops if gate=0: resumes if gate=1

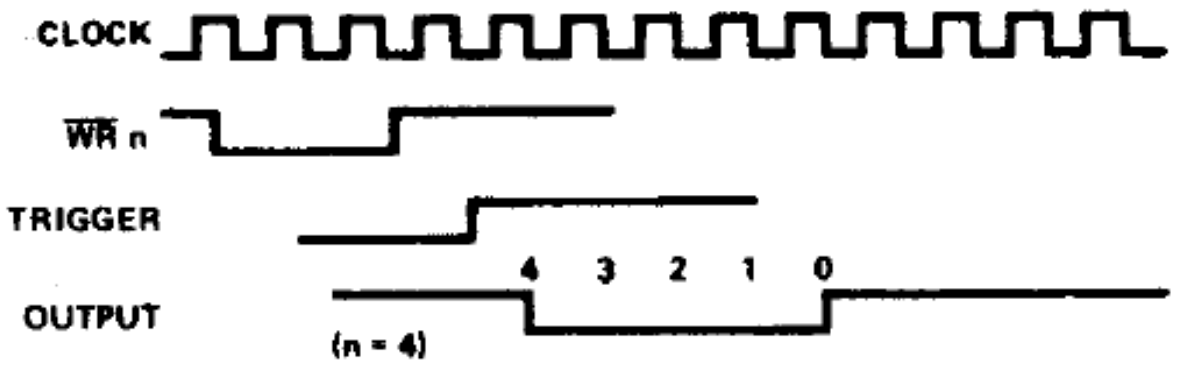
Mod 0 : Case 3



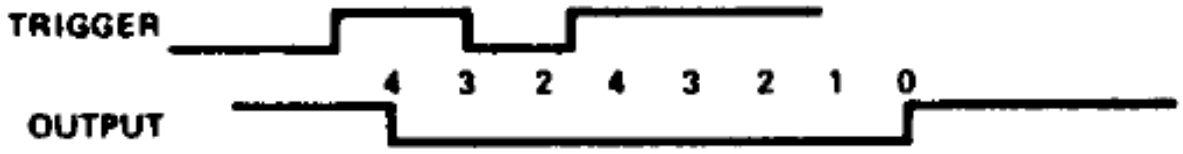
- OUT remains high till a new count is written
- Countdown continues as FF_H, FE_H if gate =1

Mode 1 –Hardware retriggerable one-shot

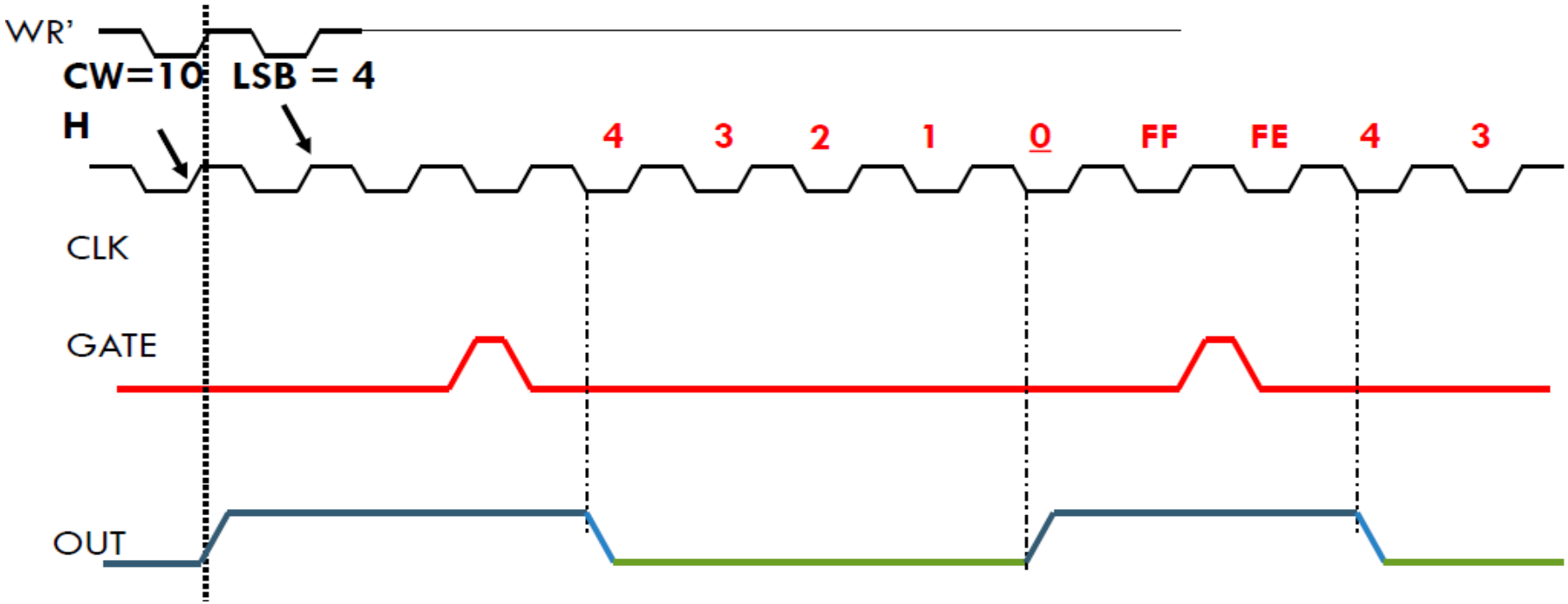
1. Output goes low following raising edge on gate
2. Output goes high when TC is reached.
3. Current output not effected by reloading count.
4. Re-triggerable



Use:
1. To create a time window for valid operations
2. Programmable pulse width.
3. To measure no activity (silence) for the given period.

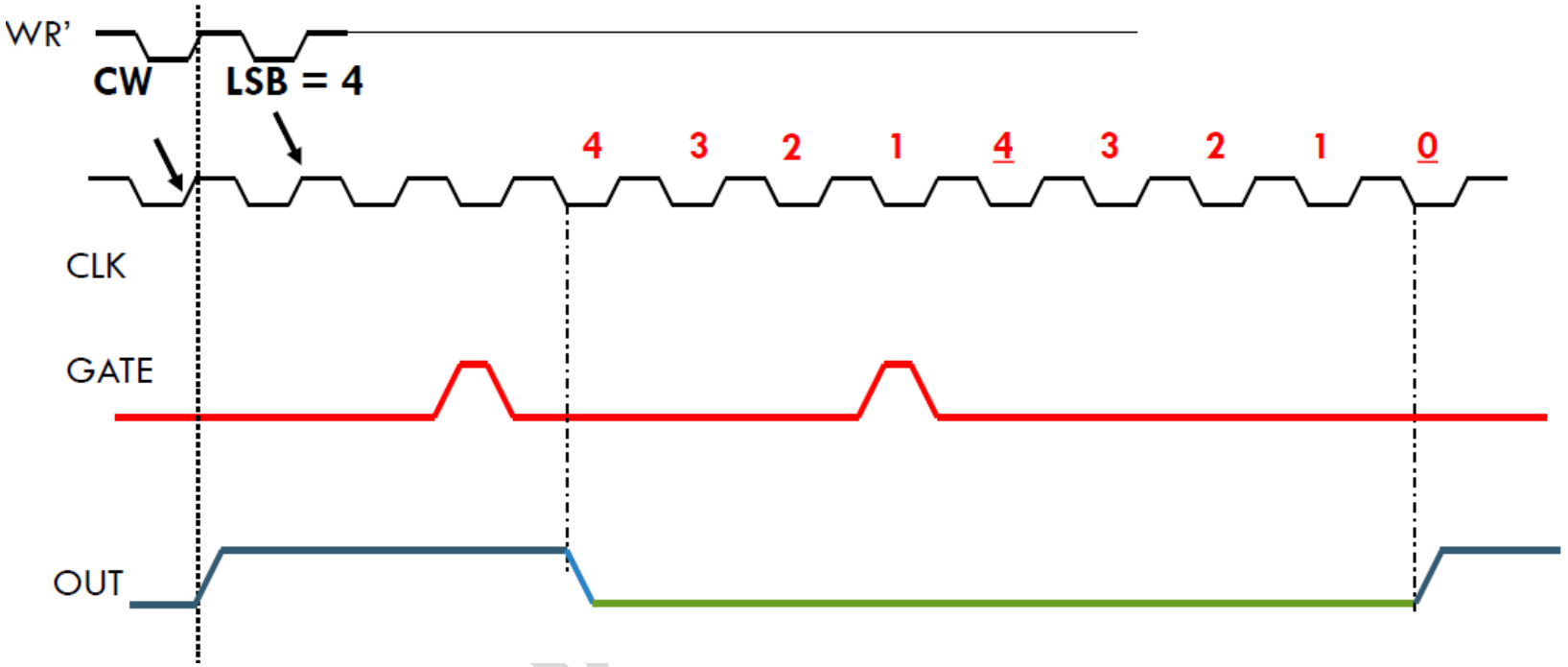


Mod 1: Case 1



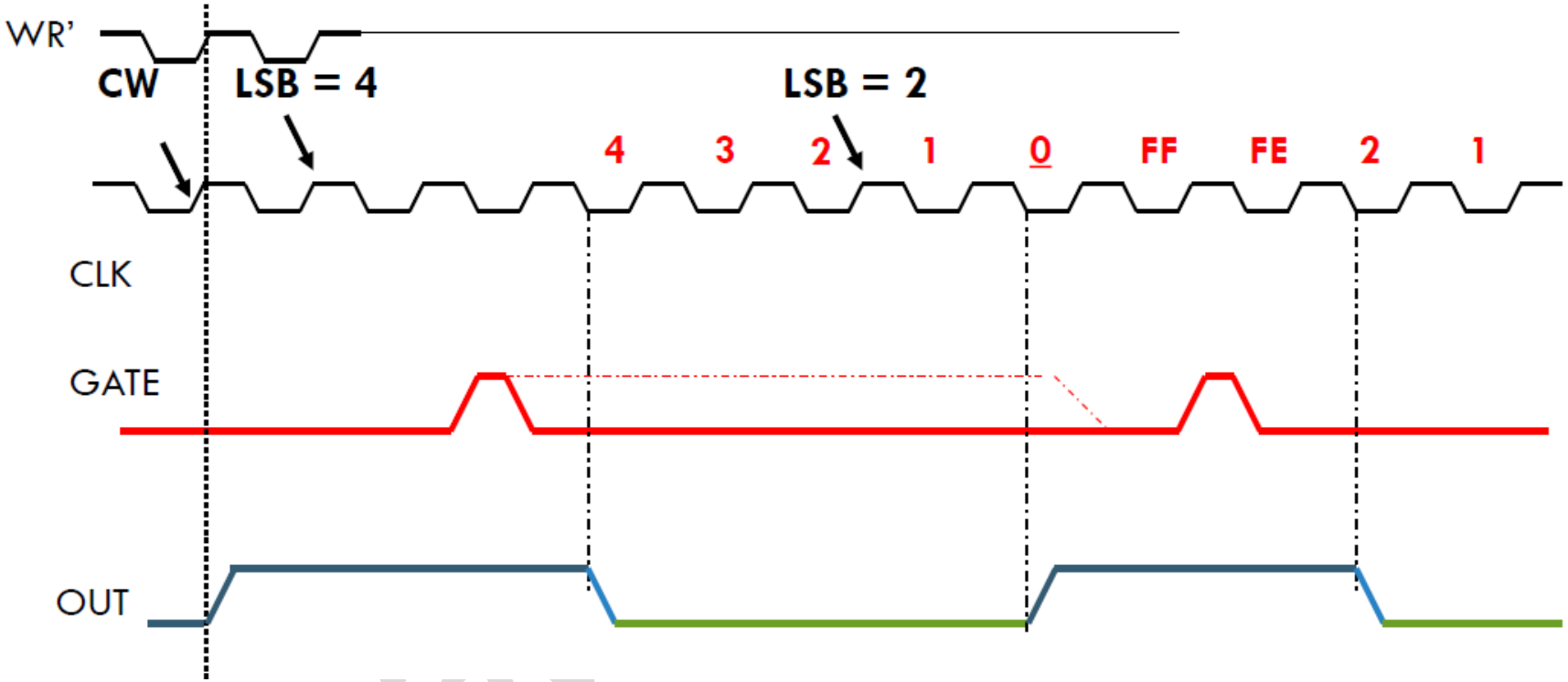
- Two step process
  - Load count register
  - Send 0-to-1 pulse on GATE to trigger it
- When triggered ⇒ o/p goes low after one clock cycle & stays low for N clock cycles ⇒ goes high

Mod 1: Case 2



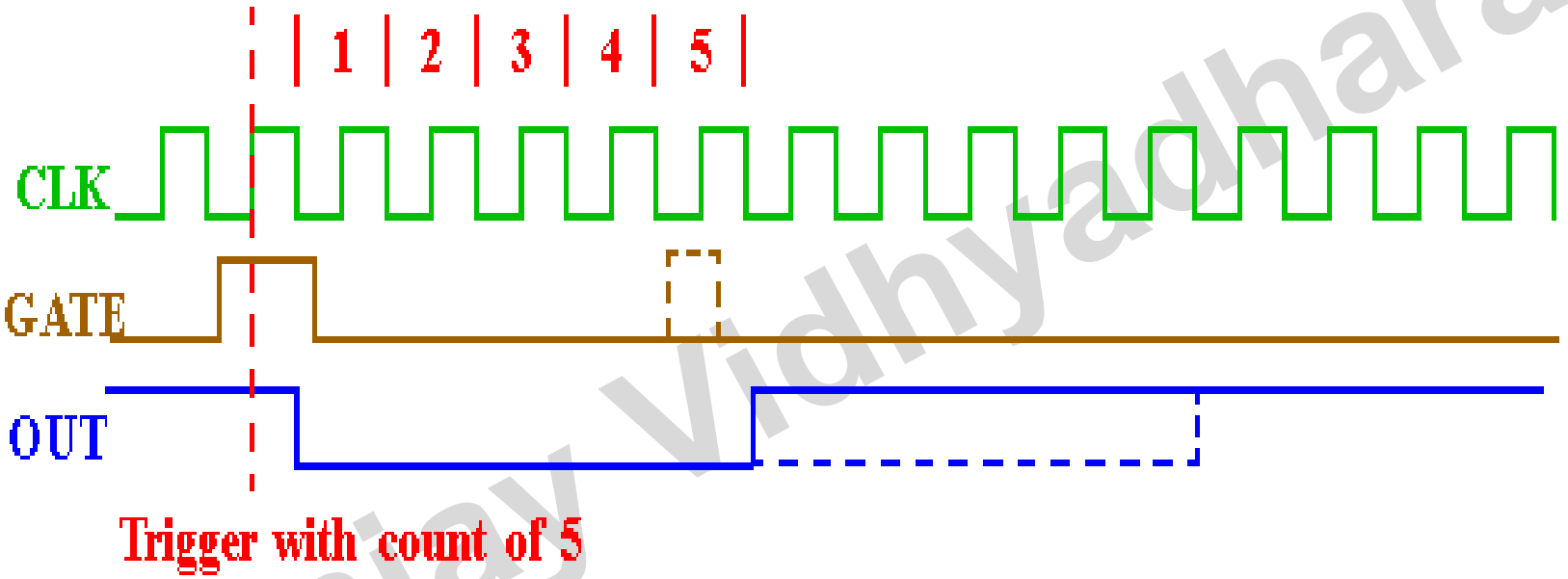
- A +ve transition at gate reloads the counter & countdown begins afresh

Mod 1: Case 3



- A new count is not loaded till gate is triggered

Modes of counting : Mode 1



Thank You