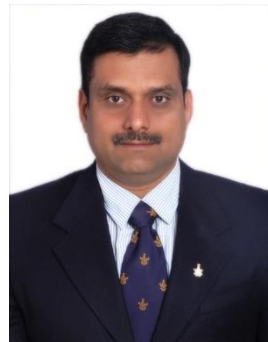




Microprocessors and Interfaces: 2021-22

Lecture 24 : 8086 Bus Cycle and Loop Delay Calculations

By Dr. Sanjay Vidhyadharan



Bus Cycle

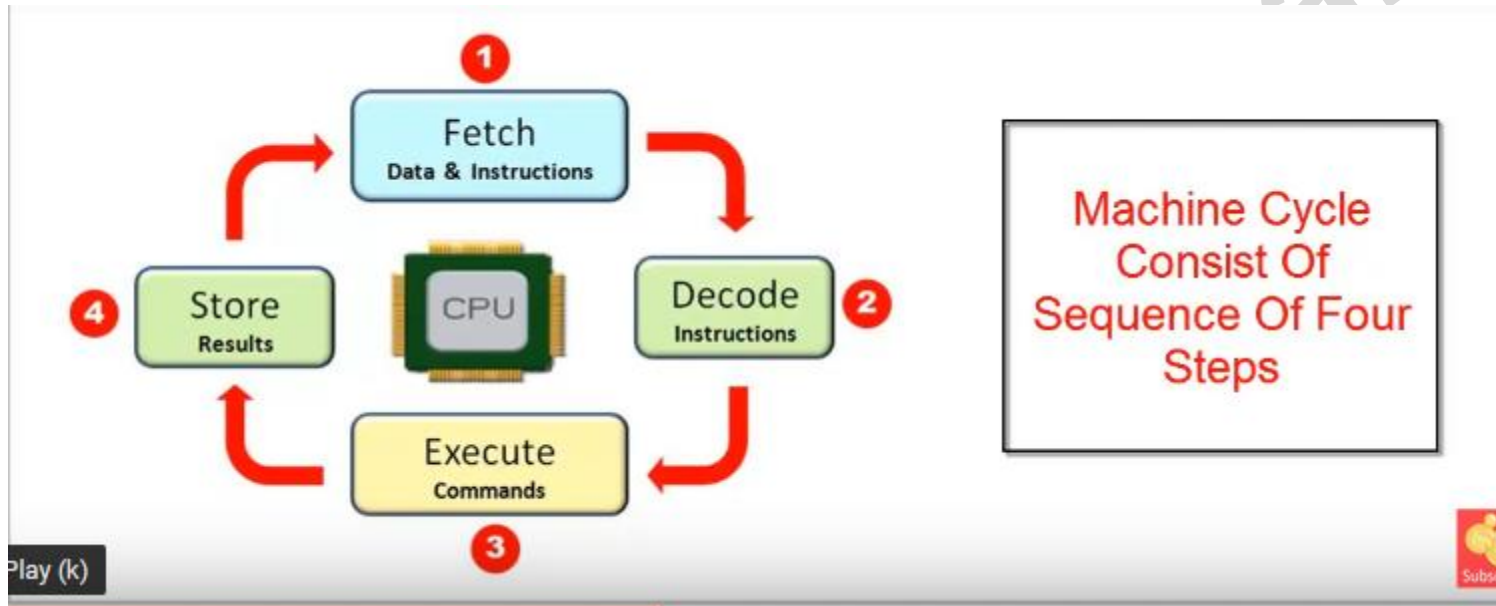
Instruction Cycle

Machine Cycle

T states

Bus Cycle

Machine Cycle



Bus Cycle

Instruction Cycle

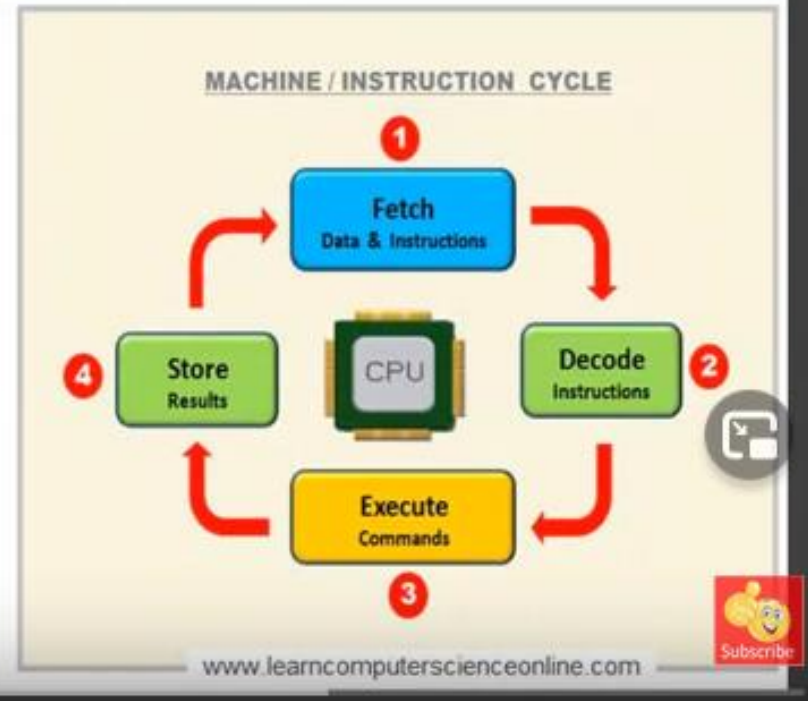
Has more than 1 Machine Cycles

CPU - Instruction Cycle / Machine Cycle .

The CPU's instruction cycle is executed sequentially and each instruction is processed by CPU which consist of following steps :

- Read an Instruction from memory .
- Decode the instruction as per OPCODE
- Find the address of operand .
- Retrieve an operand .
- Perform the desired operation
- Find the address of destination memory .
- Store the result into the destination memory

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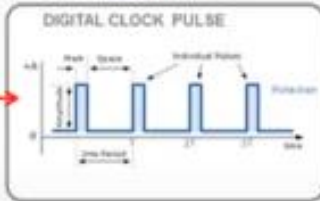
Bus Cycle

T states

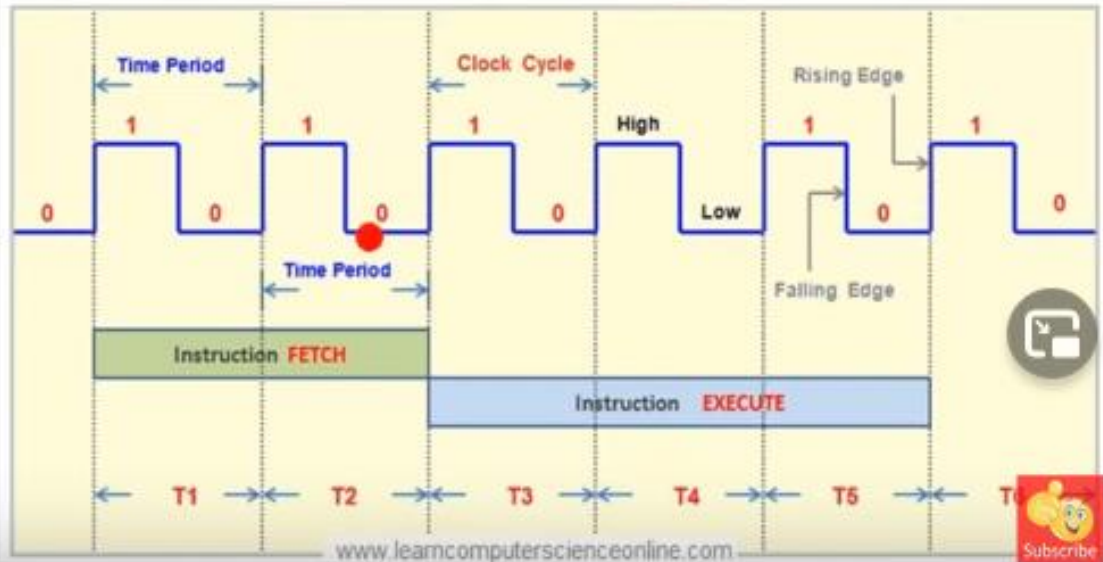
CPU – The Is Driven By Stream Of Clock Pulses

CPU AND DIGITAL CLOCK PULSE

DIGITAL CLOCK PULSES DRIVE CPU FOR EACH PULSE CPU EXECUTES A PART OF THE INSTRUCTION



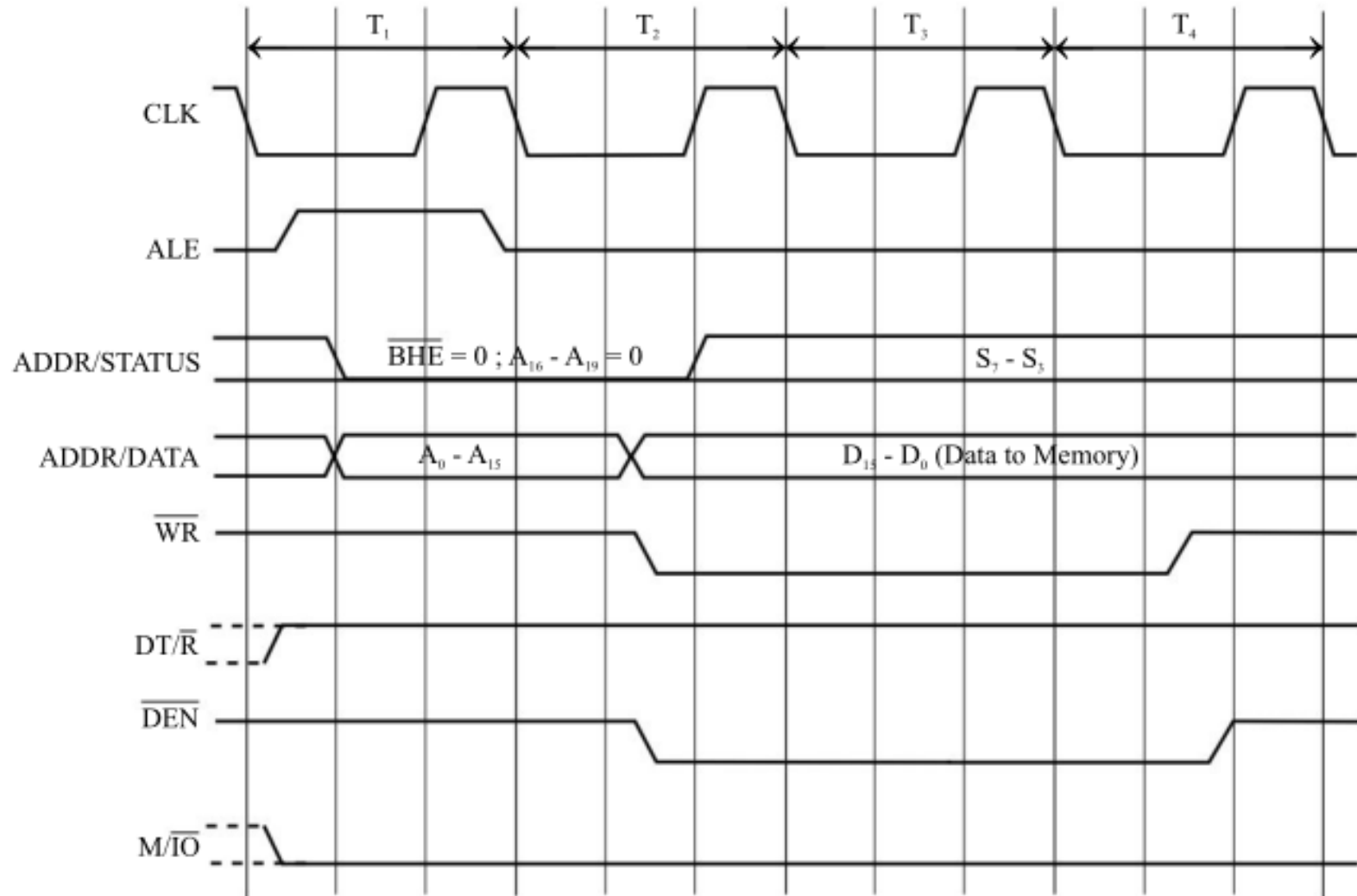
The System Clock Speed And Instruction Cycle



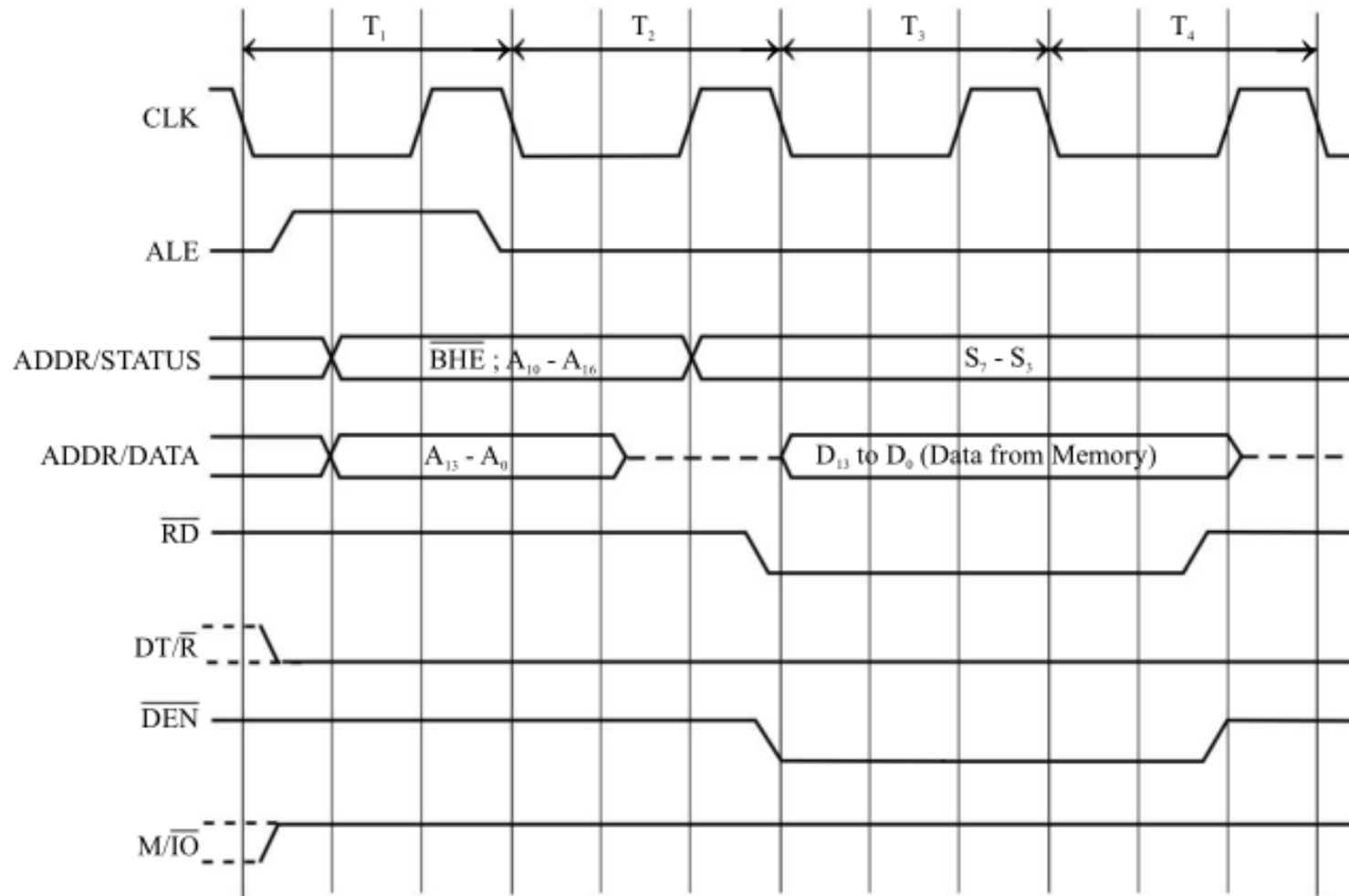
MACHINE CYCLES OF 8086

1. Opcode fetch cycle (4T)
2. Memory read cycle (4 T)
3. Memory write cycle (4 T)
4. I/O read cycle (4 T)
5. I/O write cycle (4 T)

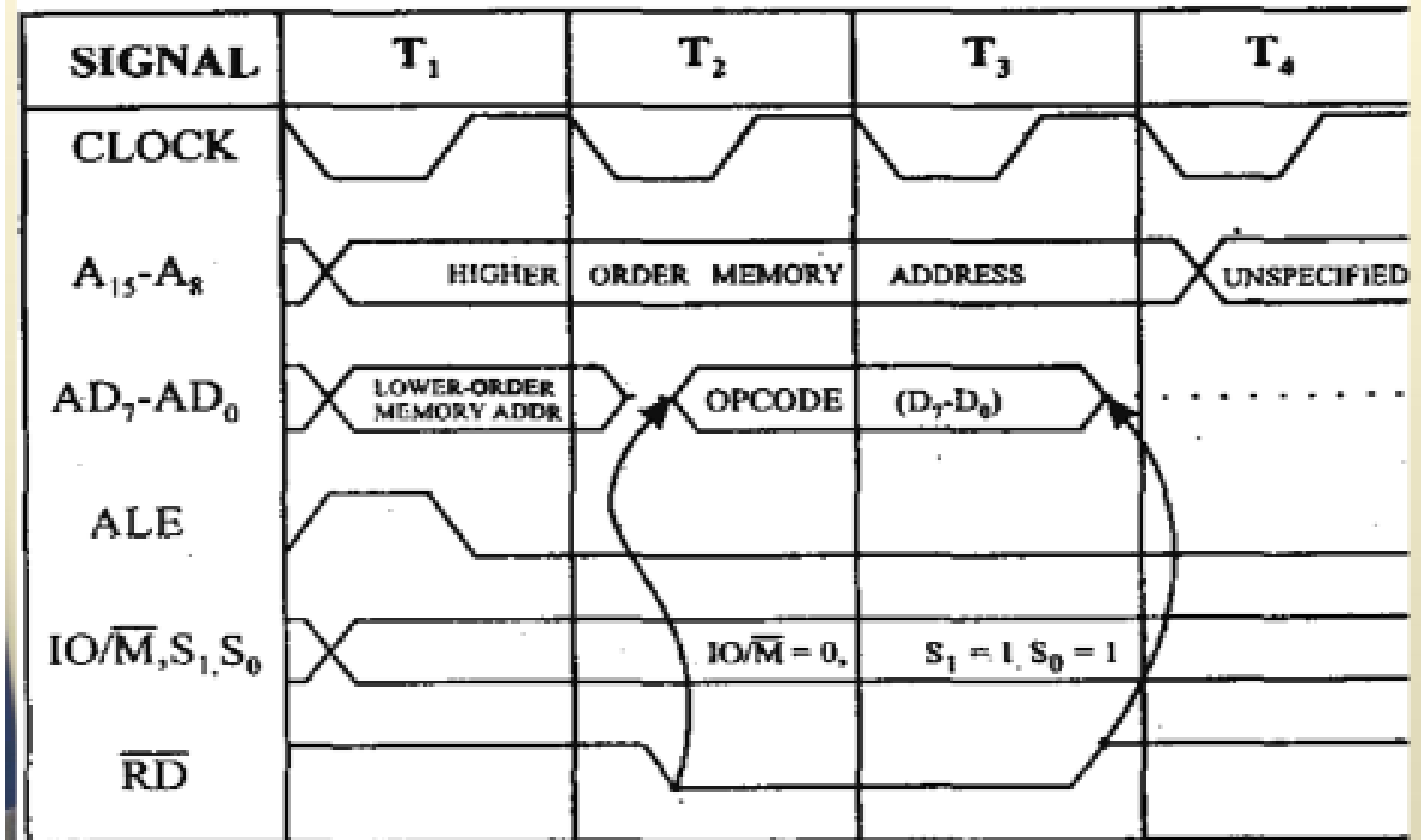
Memory Write Operation



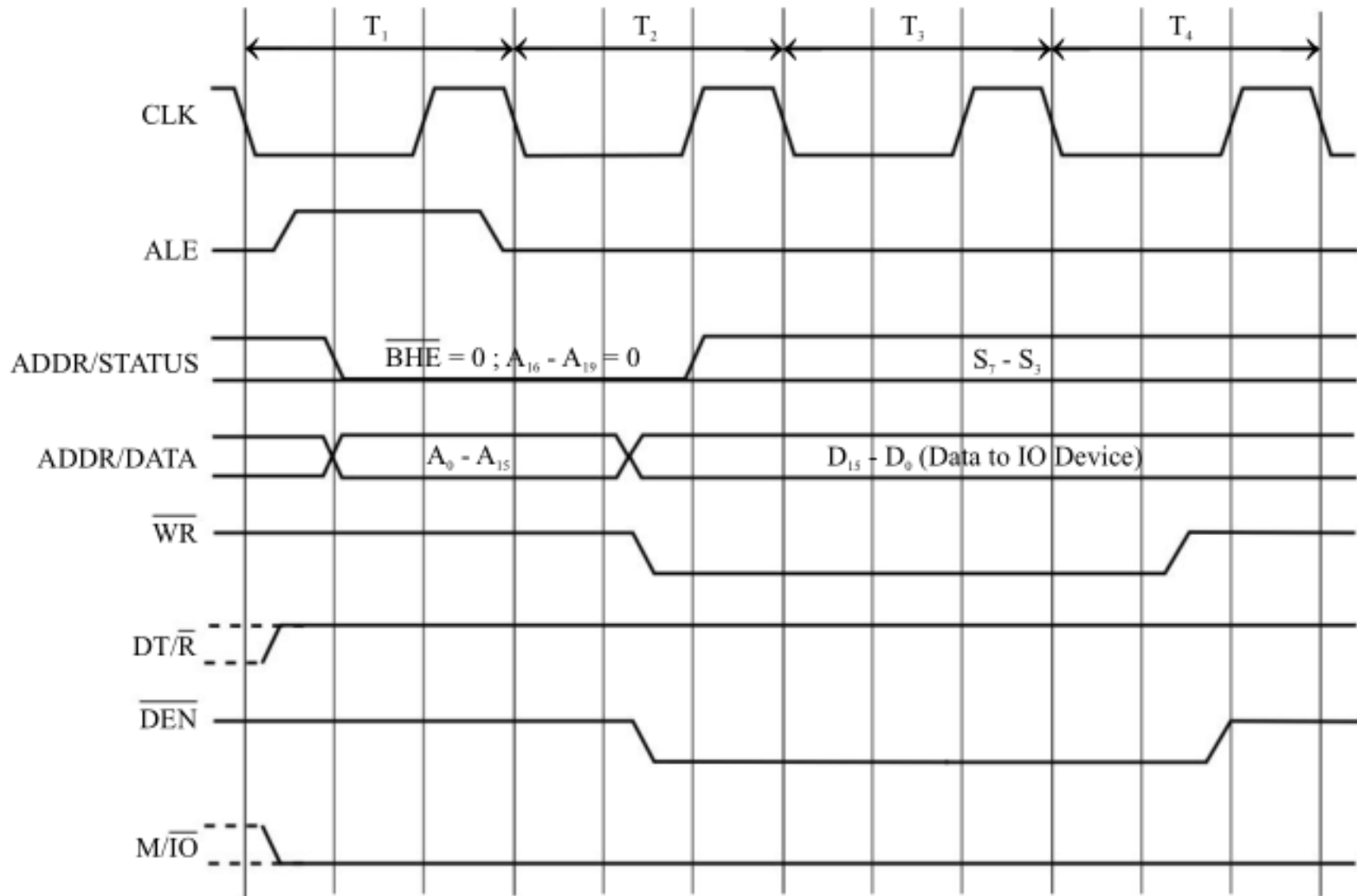
Memory Read Operation



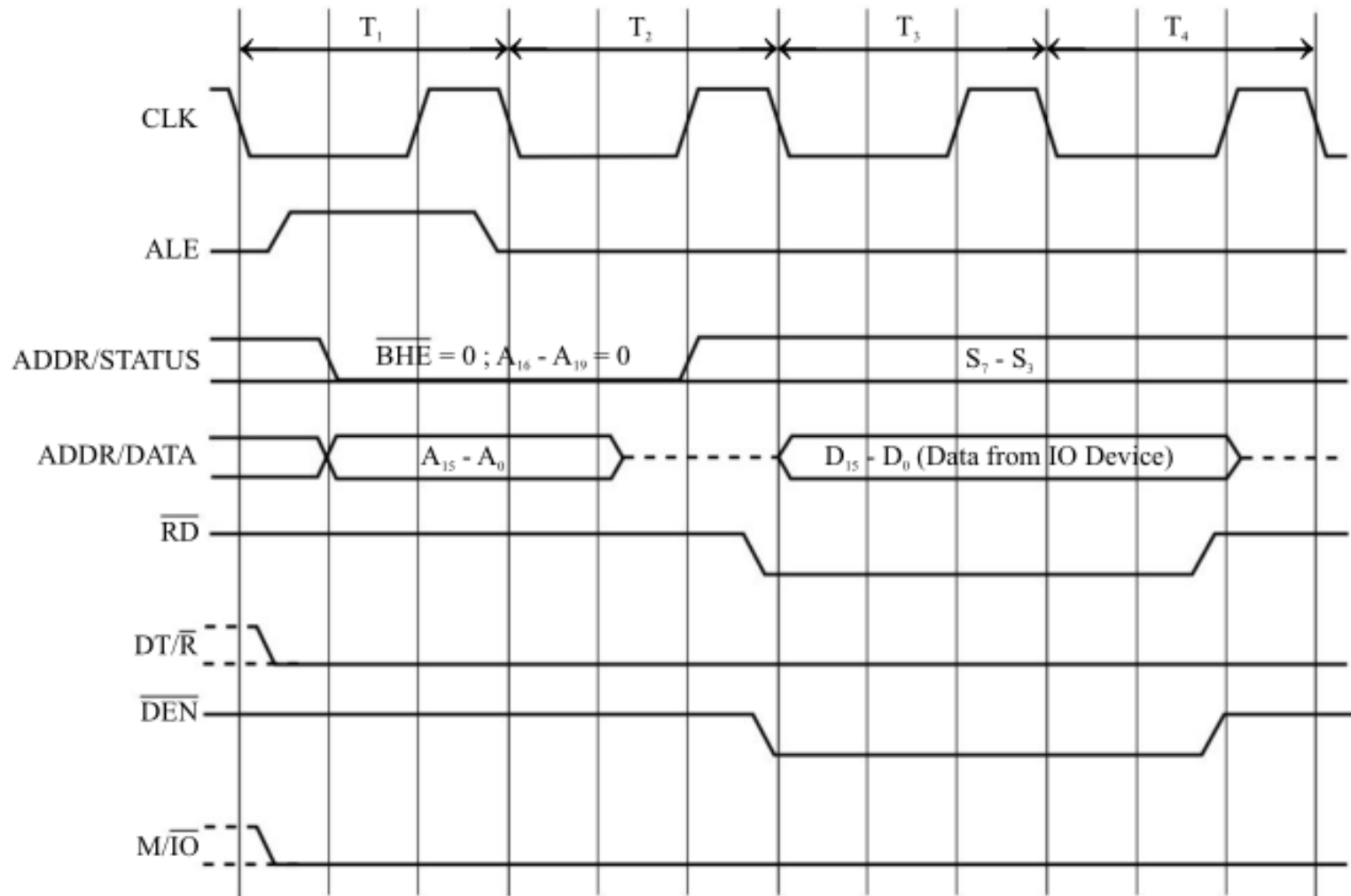
OPCODE FETCH MACHINE CYCLE



IO Write Operation



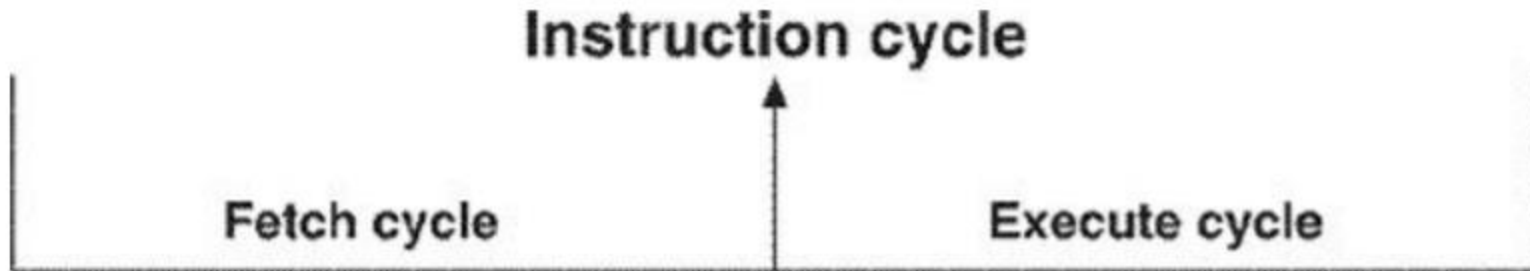
IO Read Operation



Instruction Cycle

Time taken by processor to execute an instruction- specified in terms of no. clock cycles needed to do it.

Once instruction is fetched and ready to be executed, then it can be decoded and execution can be set.



- Control unit obtains an instruction from memory
- The instruction is decoded
- Memory is given the address of the operand to be used

- Operand is obtained from memory
- Operation is performed on operands

FETCH CYCLE

Rules to identify number of machine cycles in an instruction:

1. If an addressing mode is direct, immediate or implicit then No. of machine cycles = No. of bytes/Word.

E.g. INC AX **40h** , PUSHF **9Ch** , POP AX **58H**

E.g. MOV AX,BX **8BC3h** , MOV AX,[2001h] **A10120h**

2. If the addressing mode is indirect then No. of machine cycles = No. of Words + 1.

E.g. MOV AX,[BX] **8B07h (Machine cycles = 01+1)**

Instruction Cycle

No	Instruction	No of clock cycles for execution
1	MOV AX, BX	2
2	ADD AX, BX	2
3	MUL BX	133
4	MOV BX, N	4
5	CMP AX, [BX][SI]	9+ EA
6	JNZ label	16/4
7	LOOP Label	17/5

Bus Cycle

Bus Cycle : No of Machine Cycles required for execution of the Instruction

- **MOV AX, BX**
- **8B C3**
- **1 MEMR (OPCODE FETCH)**

Bus Cycle

Bus Cycle : No of Machine Cycles required for execution of the Instruction

- **ADD BX, [0110]**
- **03 1E 10 01**
- **2 MEMR (OPCODE FETCH)**
- **i.e. 2 Machine cycles**
- **To execute the instruction**
- **1 Machine cycle---- Read Data from [0110]**
- **Total 3 Machine Cycles**

Bus Cycle

Bus Cycle : No of Machine Cycles required for execution of the Instruction

- **ADD [0110], BX**
- **01 1E 10 01**
- **To instruction fetch:**
- **2 MEMR (OPCODE FETCH)**
- **2 Machine cycle**
- **To execute the Instruction**
- **1 Machine cycle---- Read Data from [0110]**
- **1 Machine cycle---- Store Results in DS:0110**
 –(1 MEMW)
- **Total 4 Machine Cycles**

Bus Cycle

Bus Cycle : No of Machine Cycles required for execution of the Instruction

- **CBW**
- **98**
- **1 MEMR (OPCODE FETCH)**

DELAY LOOPS

Certain amount of time or delay is associated with the execution of an Instruction.

- Thus instruction execution gives us a means of generating a delay . Consider instructions below,

MOV CX, 100	4 cycles
HERE: LOOP HERE	17/5 cycles

- Total no. of clock cycles required is $4 + (100 * 17) - 12 = 1692$ cycles
- In a system with 12 MHz clock, clock period is $.083 \mu \text{ Sec}$
- Total delay in this case $.083 * 1692 = 140 \mu \text{ Sec}$
- It is possible to fix the value of N so as to get a desired value of delay .

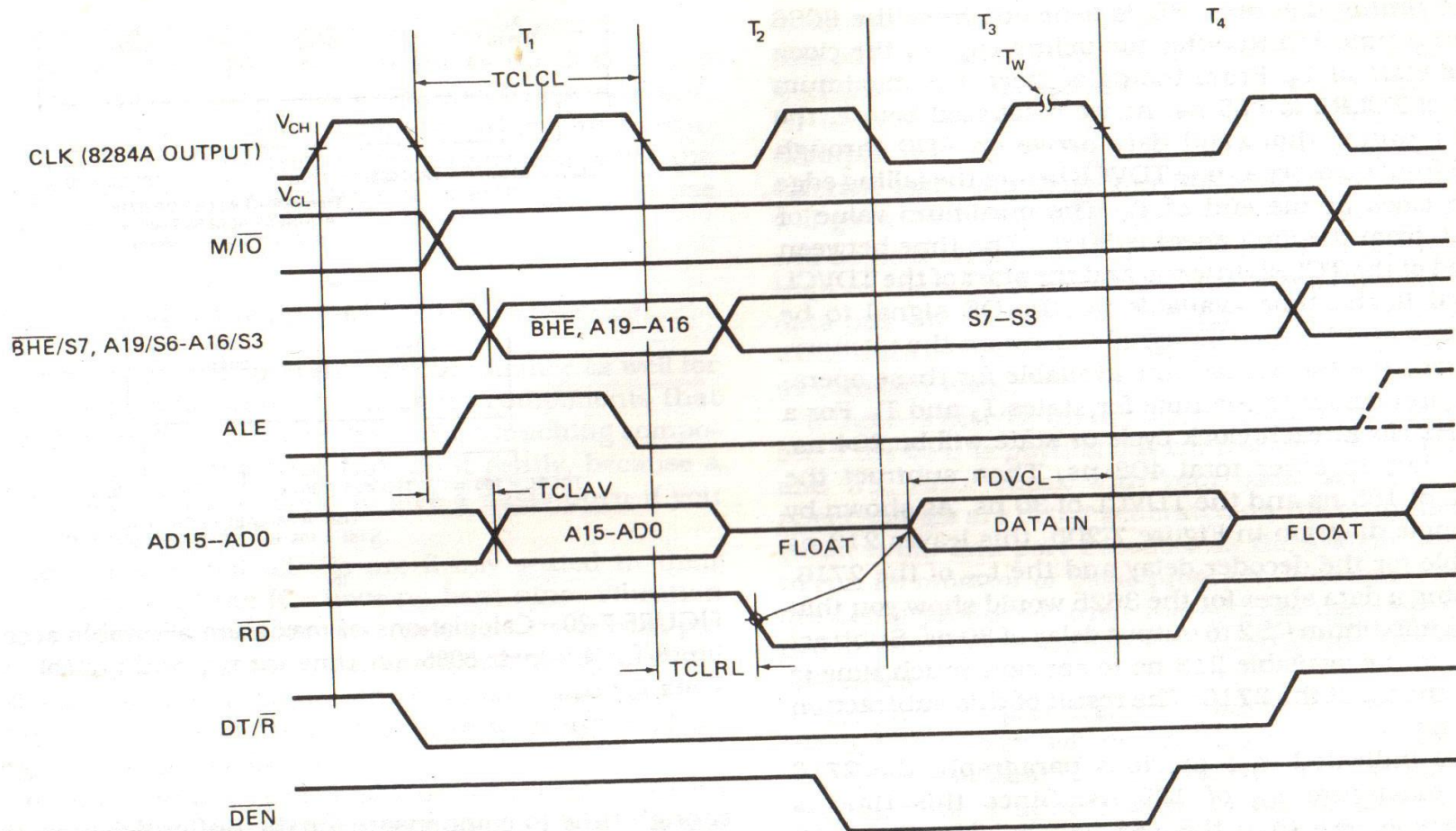
DELAY LOOPS

MOV CX,N	4
HERE: NOP	3
LOOP HERE	17/5

Most of the delay occurs within the loop
the total cycles of delay is $=(3+17) \times N - 12$.

- Total delay time = 1 m sec = $20N \times 0.083 \mu\text{secs}$
- For 1 msec delay ,the value of N =602 or 25AH
- This value of N is inserted into program to create a delay of 1msec
- Generating delays in this manner is called software delays.

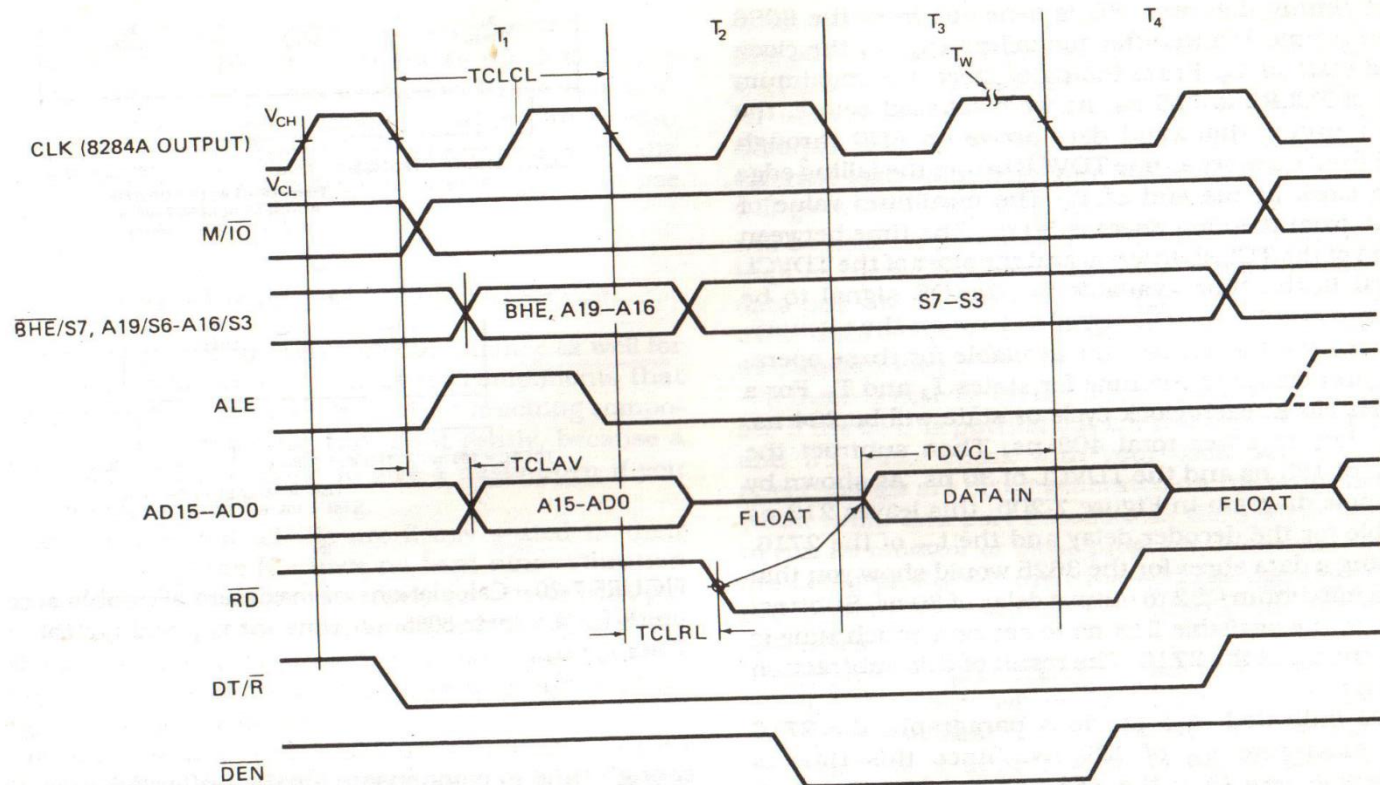
MEMORY ACCESS TIME



TCLAV- Time from Clock to Address Valid ; 110 ns for MHz Clock

Memory Access Time : TCLAV time must be subtracted from the three clocking states (600 ns) separating the appearance of the address (T_1) and the sampling of the data (T_3).

MEMORY ACCESS TIME



- TCLRL- Time from Clock to Read Line
- TDVCL – Time Data Valid to Clock 30ns
- Memory Access Time : 600 ns-110ns-30ns = 460 ns
- A wait state (T_w) is an extra clocking period between T_2 and T_3 to lengthen bus cycle
- On one wait state, memory access time of 460 ns, is lengthened by one clocking period (200 ns) to 660 ns, based on a 5 MHz clock.

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- Thankyou

Sanjay Vidnyadhharan