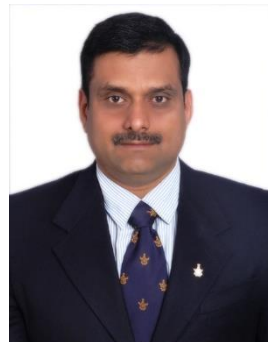




Microprocessors and Interfaces: 2021-22

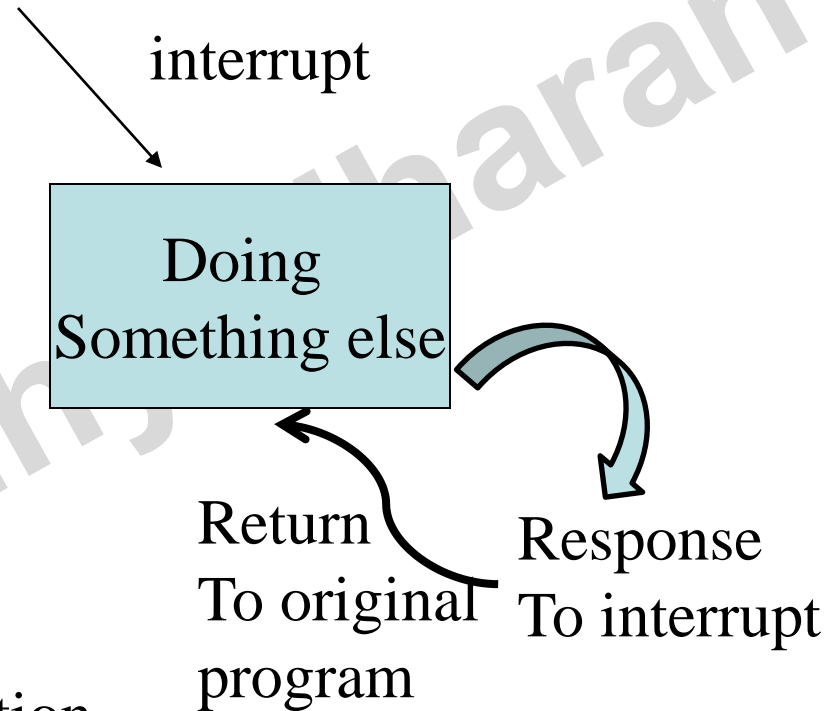
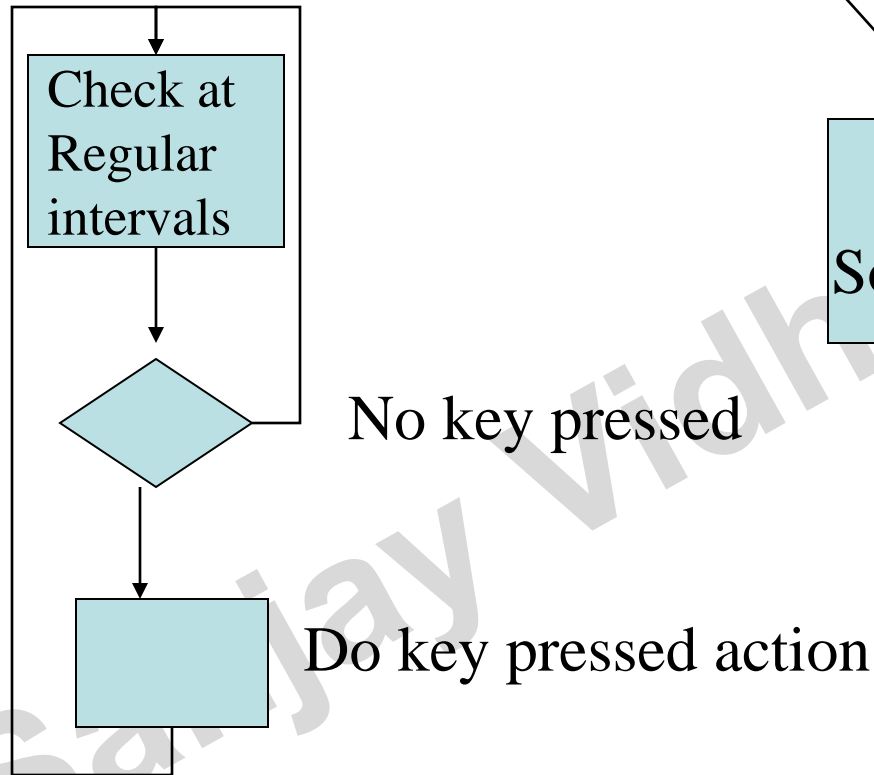
Lecture 21 : Interrupts

By Dr. Sanjay Vidhyadharan

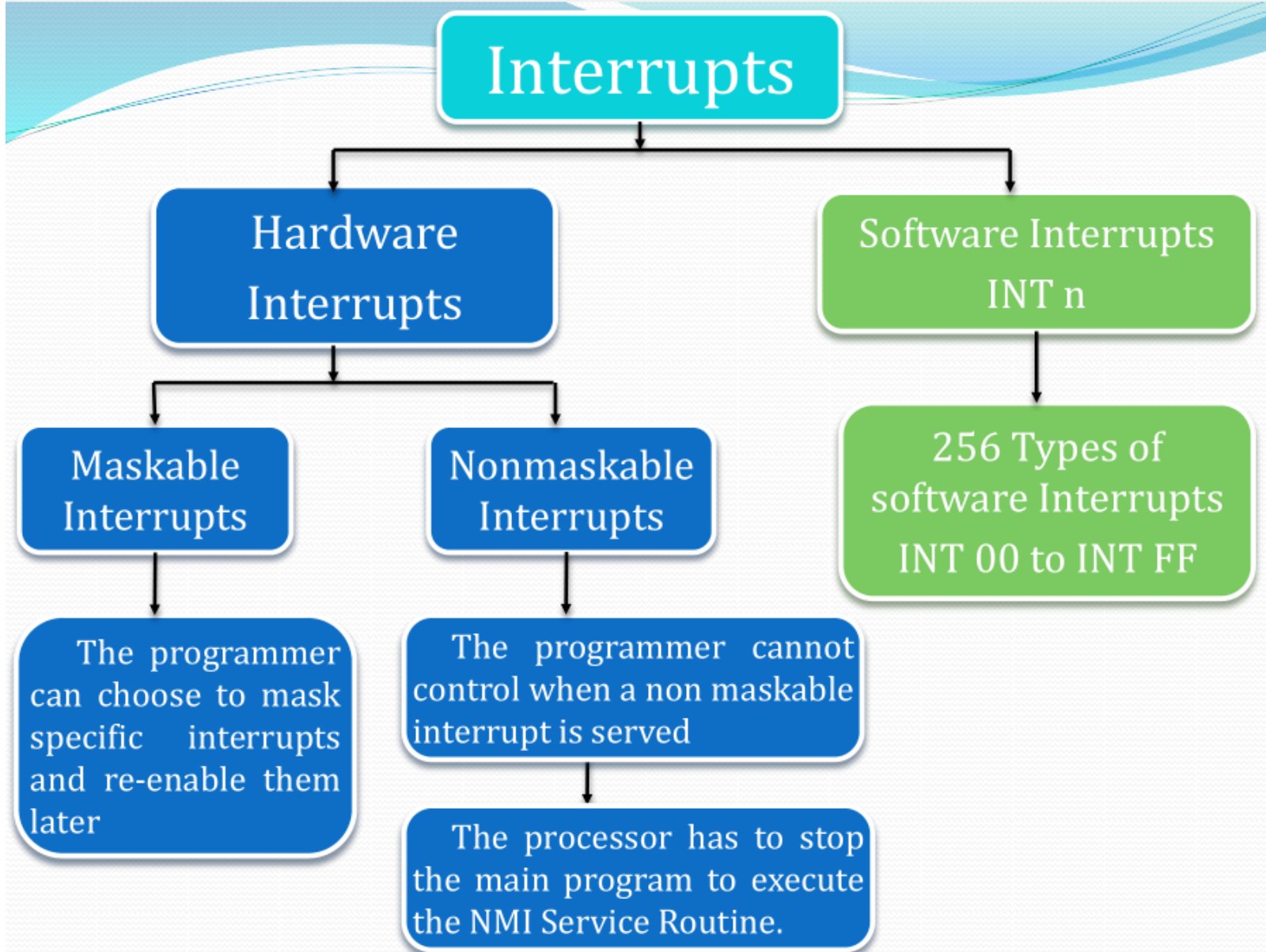


Interrupts vs. Polling

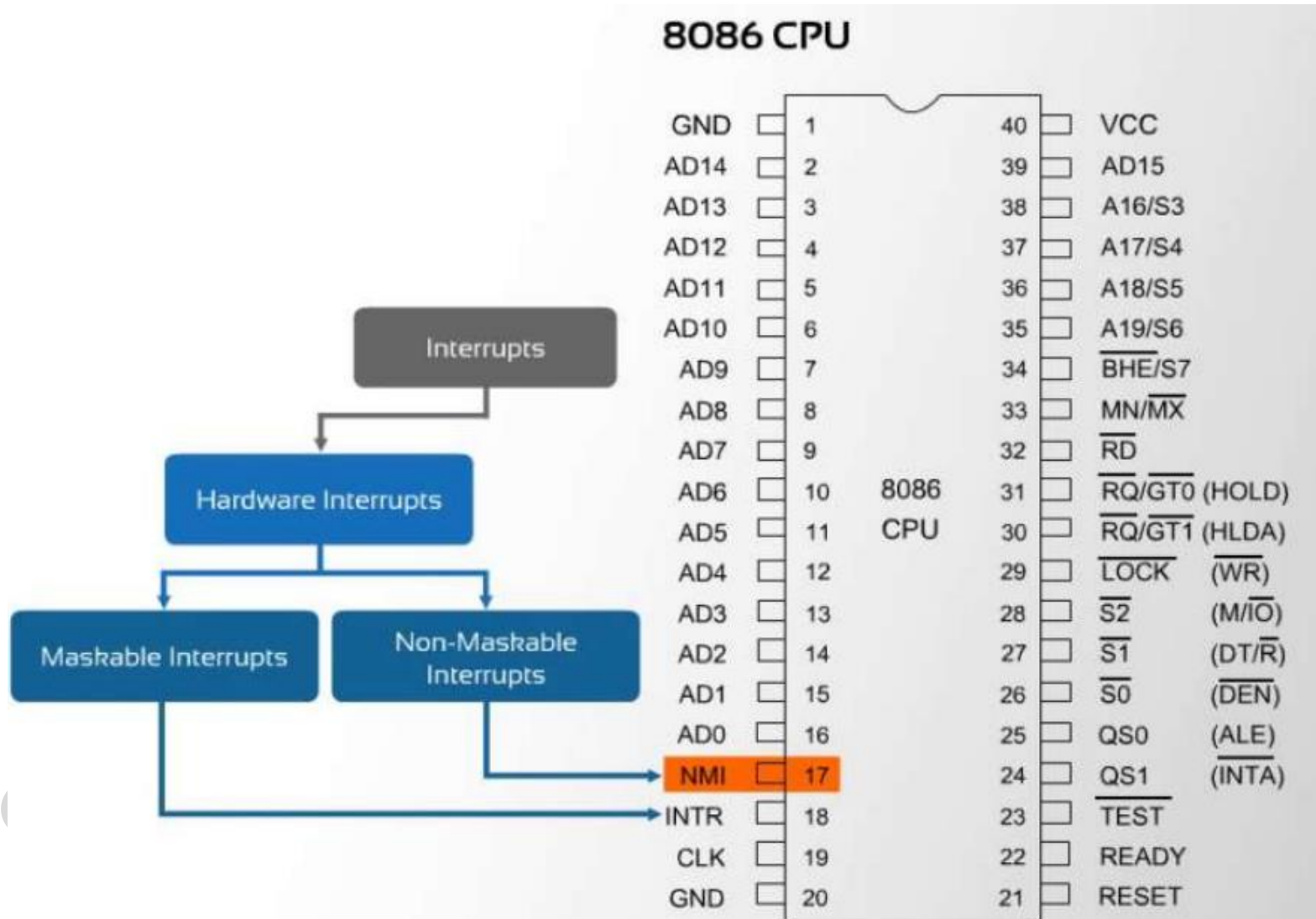
Polling



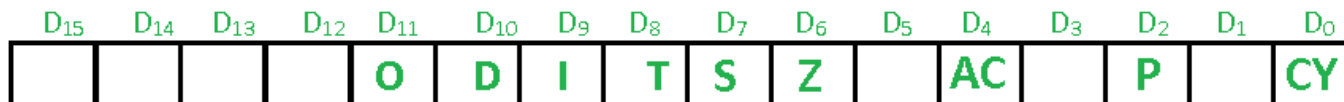
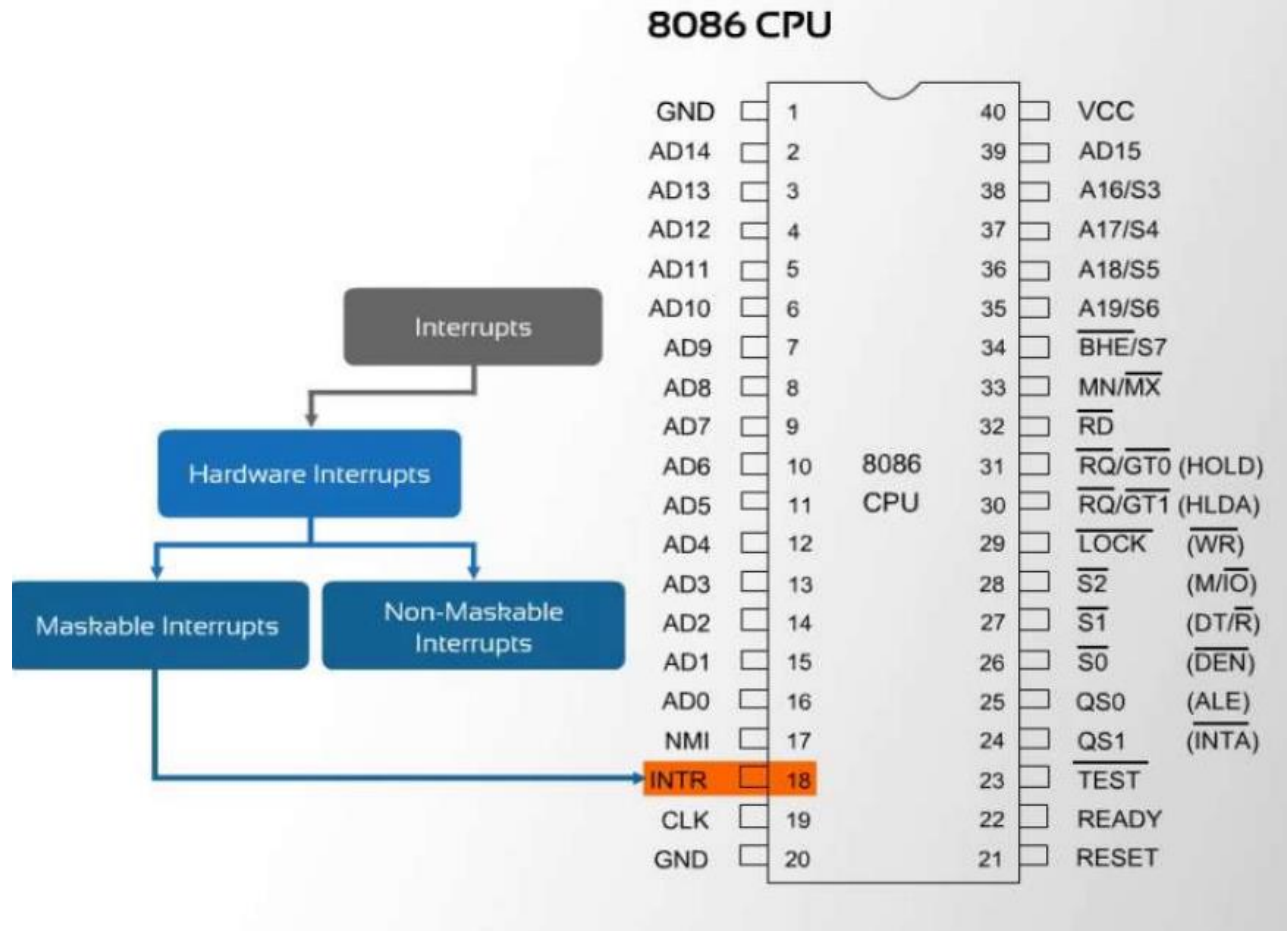
Types of 8086 Interrupts



8086 Interrupts



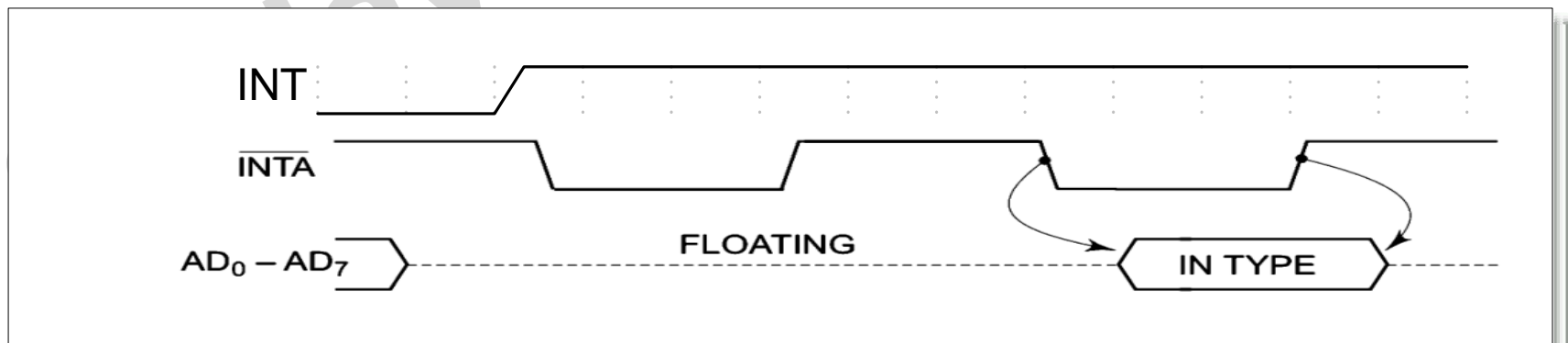
8086 Interrupts



Hardware Interrupts : Interrupt pins and timing

x86 Interrupt Pins

- **INTR**: Interrupt Request. Activated by a peripheral device to interrupt the processor.
 - Level triggered. Activated with a logic 1.
- **/INTA**: Interrupt Acknowledge. Activated by the processor to inform the interrupting device that the interrupt request (INTR) is accepted. **(IF Checked)**
 - Level triggered. Activated with a logic 0.
- **NMI**: Non-Maskable Interrupt. Used for major system faults such as parity errors and power failures.
 - Edge triggered. Activated with a positive edge (0 to 1) transition.
 - Must remain at logic 1, until it is accepted by the processor.
 - Before the 0 to 1 transition, NMI must be at logic 0 for at least 2 clock cycles.
 - **INT 02h**



8086 Vector Table

Interrupt Type	Content (16-bit)	Address	Comments	
Type 0	ISR IP	0000:0000	Reserved for divide by Zero interrupt	
	ISR CS	0000:0002		
Type 1	ISR IP	0000:0004	Reserved for single step interrupt	
	ISR CS	0000:0006		
Type 2	ISR IP	0000:0008	Reserved for NMI	
	ISR CS	0000:000A		
Type 3	ISR IP	0000:000C	Reserved for INT single byte instruction	
	ISR CS	0000:000E		
Type 4	ISR IP	0000:0010	Reserved for INTO instruction	
	ISR CS	0000:0012		
Type N		0000:0014	Reserved for two byte instruction INT TYPE	
		0000:0016		
	ISR IP	0000:004N		
	ISR CS	0000:(004N+2)		
		0000:03FC		
	Type FFH	ISR IP		0000:03FE
		ISR CS		0000:03FF

ISR: Interrupt Service Routine

INT 0

The screenshot shows the emu8086 emulator interface. The main window displays assembly code with the following instructions:

```
01  
02 ; You may customize the location of the interrupt vector table  
03 ; The location of the interrupt vector table is 0000:0000  
04  
05 org 100h  
06  
07 Mov BL, 00h  
08 Mov AL, 01h  
09 Div B1  
10 Hlt  
11  
12 ret  
13  
14  
15  
16  
17
```

A message box titled "message" is overlaid on the screen, displaying the following text:

divide error - overflow.
to manually process this error,
change address of INT 0 in interrupt vector table.

The message box has an "OK" button at the bottom.

The emulator's status bar at the bottom shows the following memory addresses and values:

F417A:	00	000	NULL
F417B:	00	000	NULL

Interrupt Sub-Routine (ISR)

256 Interrupts Of 8086 are Divided in To 3 Groups

1. Type 00 to Type 04 interrupts-

These are used for fixed operations and hence are called dedicated interrupts

2. Type 05 to Type 31 interrupts

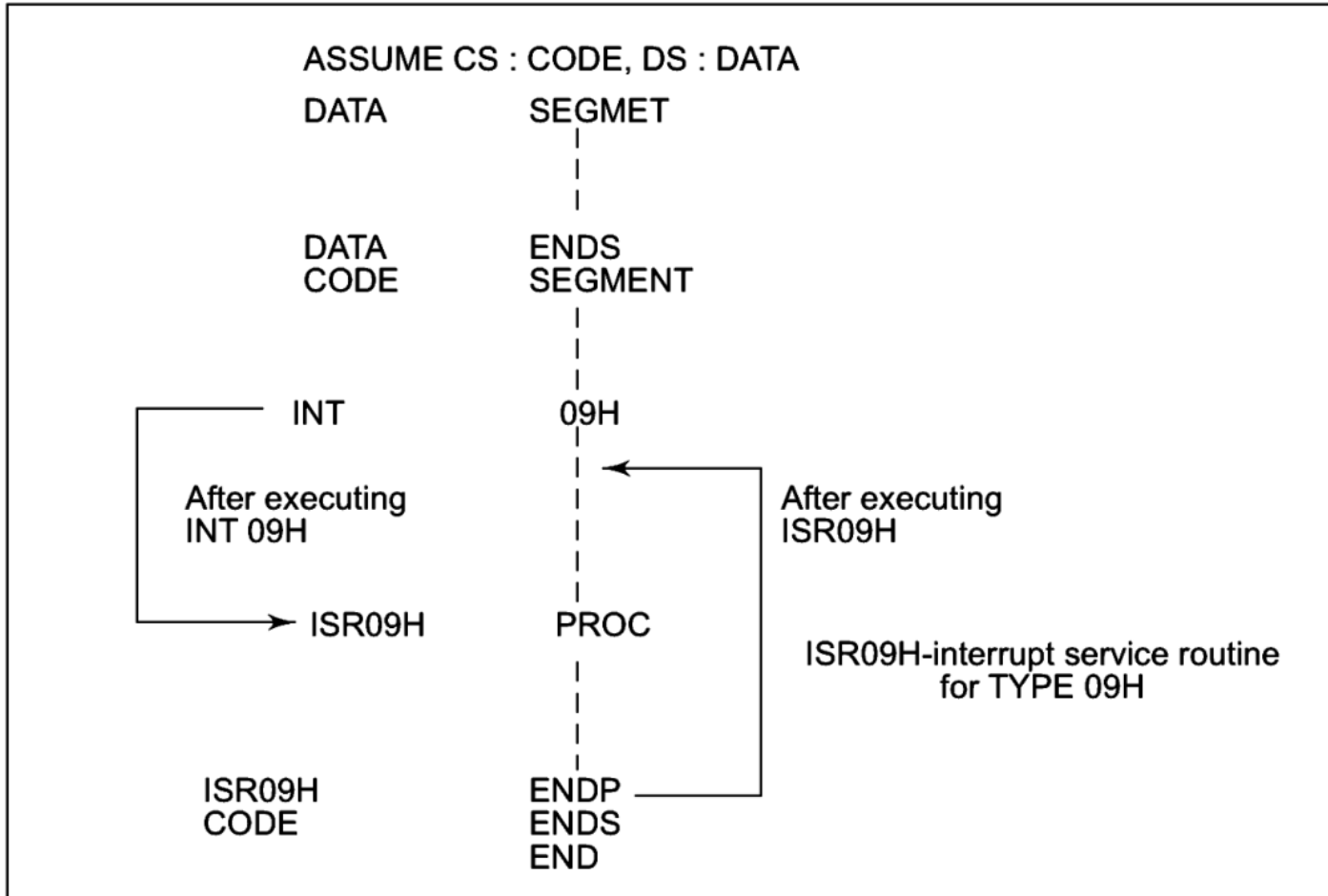
Preserved for Higher processors

3. Type 32 to Type 255 interrupts

Available for user, called user defined interrupts these can be H/W interrupts and activated through INTR line or can be S/W interrupts.

[E.g. int 21 : 34th interrupt in vector Table or Type 33]

Soft Interrupts 8086



Bus Cycle

Instruction Cycle

Machine Cycle

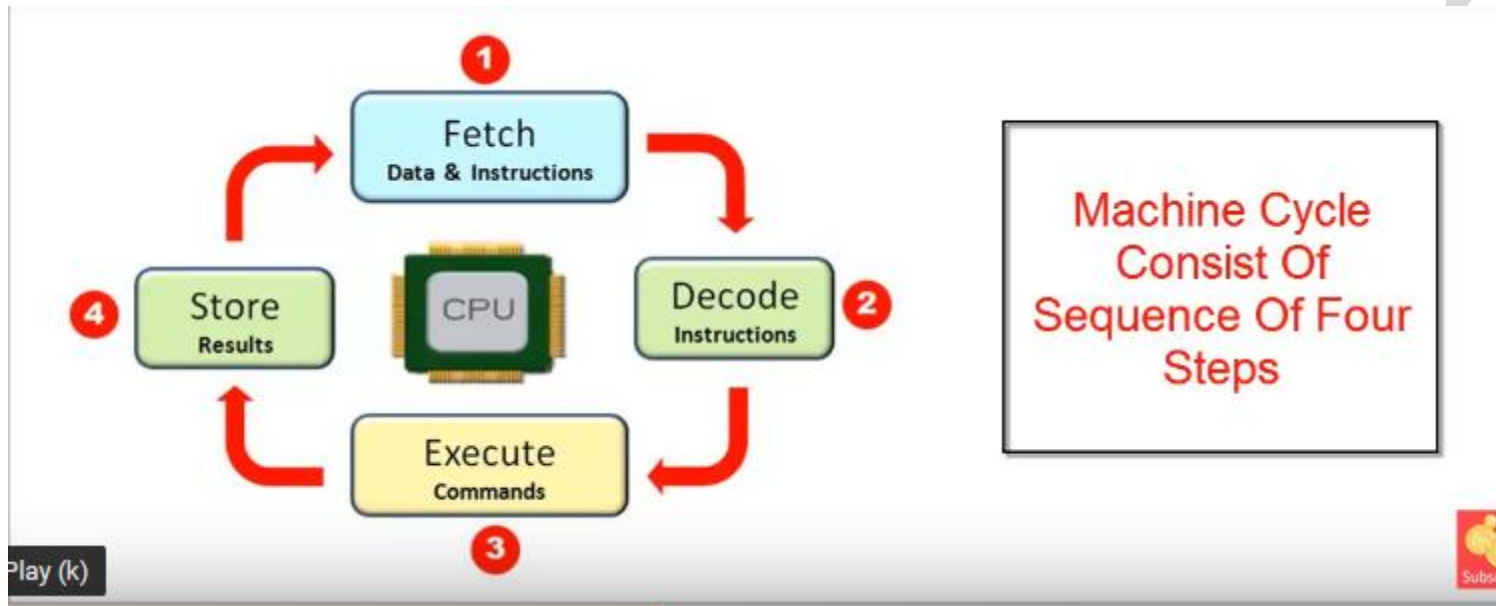
T states

Sanjay

aran

Bus Cycle

Machine Cycle



Bus Cycle

Instruction Cycle

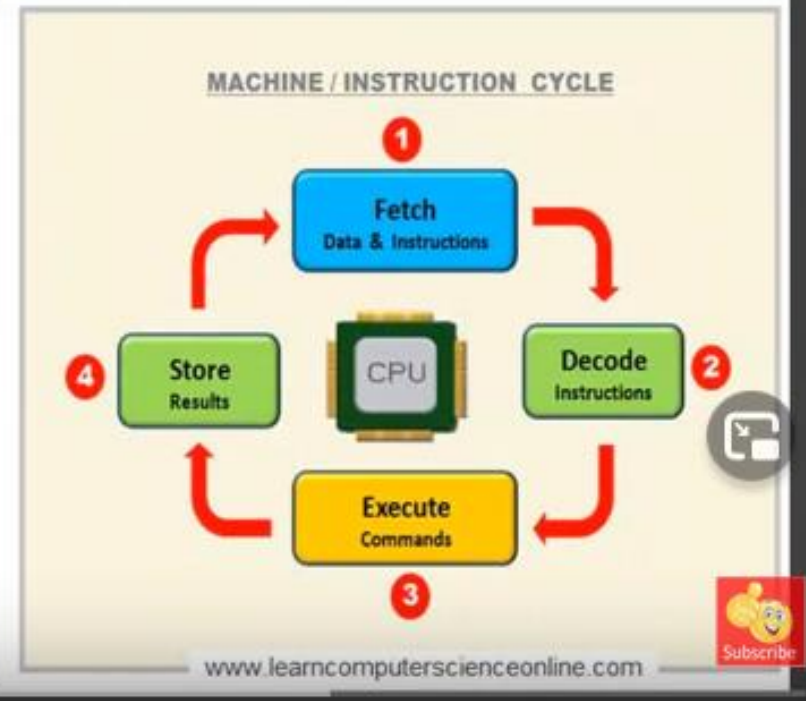
Has more than 1 Machine Cycles

CPU - Instruction Cycle / Machine Cycle .

The CPU's instruction cycle is executed sequentially and each instruction is processed by CPU which consist of following steps :

- Read an Instruction from memory .
- Decode the instruction as per OPCODE
- Find the address of operand .
- Retrieve an operand .
- Perform the desired operation
- Find the address of destination memory .
- Store the result into the destination memory

www.learncomputerscienceonline.com



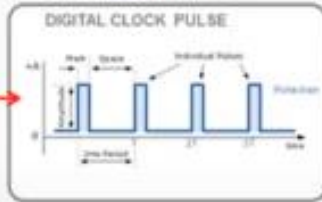
Bus Cycle

T states

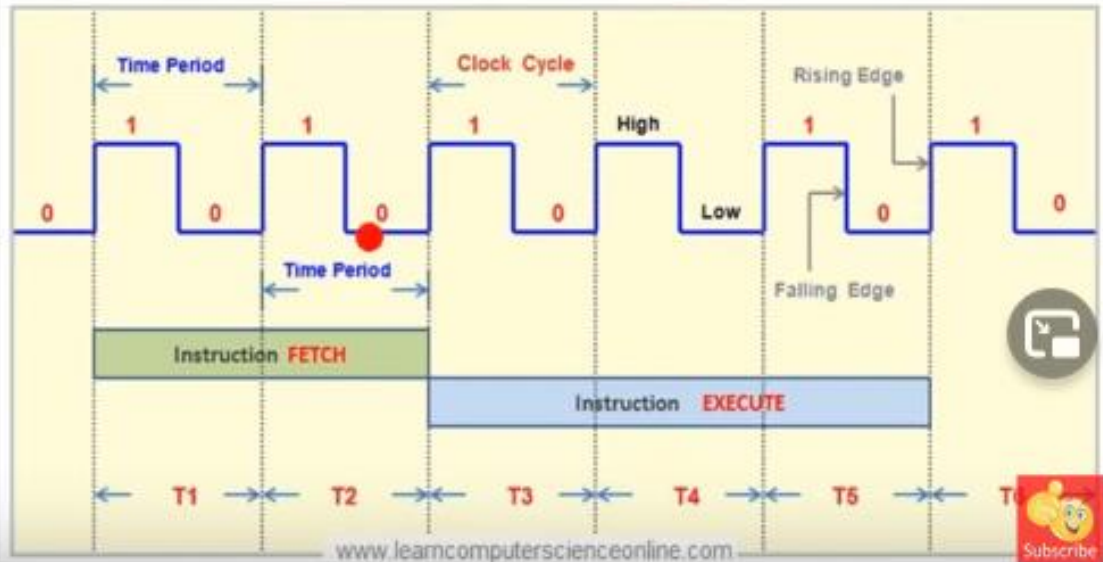
CPU – The Is Driven By Stream Of Clock Pulses

CPU AND DIGITAL CLOCK PULSE

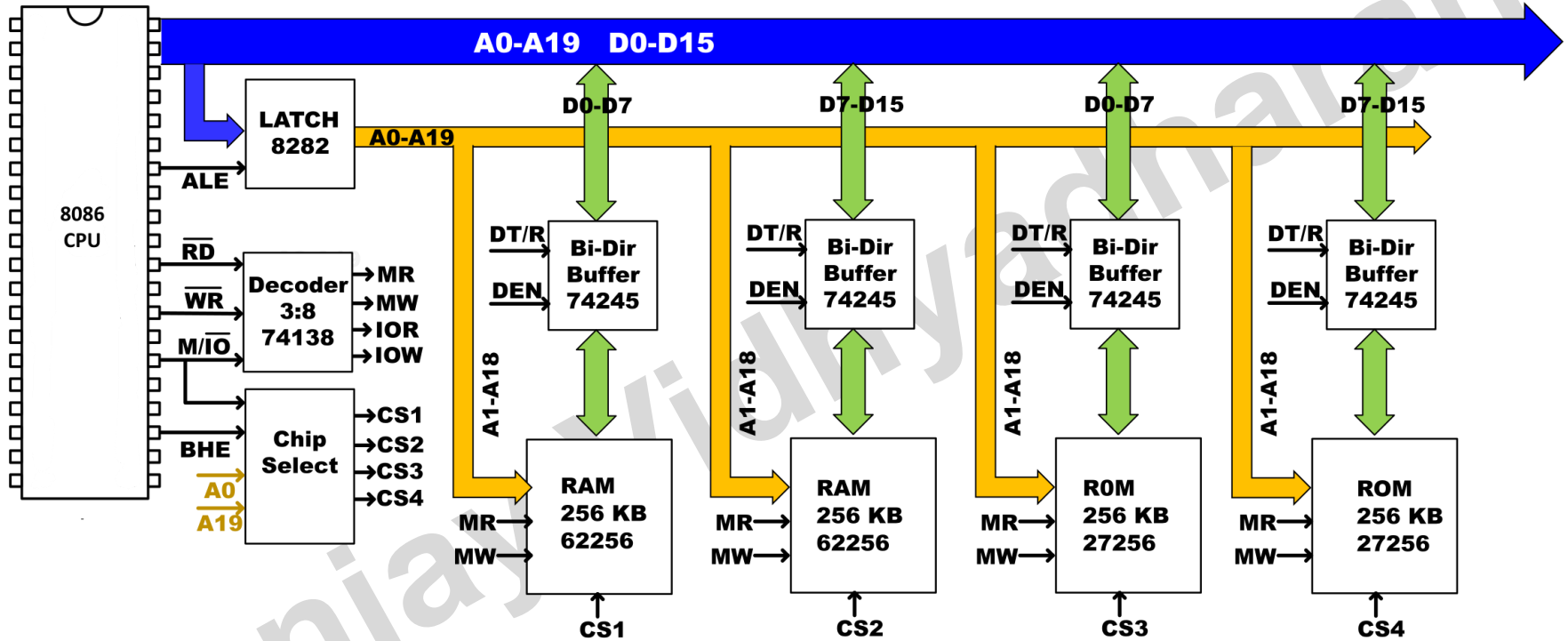
DIGITAL CLOCK PULSES DRIVE CPU FOR EACH PULSE CPU EXECUTES A PART OF THE INSTRUCTION



The System Clock Speed And Instruction Cycle



8086 Memory Interface



-
- Thankyou

Sanjay Vidhyadharan